Embedded Linux for Hot Swapping Partially Reconfigurable FPGA Cores Victor G. Lesau, William A. Gruver, and Dorian Sabaz Intelligent / Distributed Enterprise Automation Laboratory - A B

1. Project Description

Dynamic Partial Reconfiguration (PR) of Field Programmable Gate Arrays (FPGAs) is a technology that enables the development of embedded systems and allows hot swappable logic on the FPGA fabric. This means that hardware logic can be swapped in and out on-the-fly. Because PR is still relatively new, taking advantage of this technology requires working with immature tools. This project is aimed at developing FPGA tools – along with Linux – that take advantage of partial reconfiguration and make it easier to dynamically manage FPGA resources.

2. Partial Reconfigurable FPGAs and the Path Forward

FPGA without PR and External Support (Past)



Hardware cores are synthesized and loaded onto an FPGA. Management of the FPGA and its cores are done via external on-board (off FPGA) components.

FPGA with PR and External Support (Present)



Hardware cores are synthesized and loaded onto both static and dynamic parts of the FPGA. Management of the FPGA is performed by external on-board components, whereas the FPGA's dynamic cores are managed by the static part of the FPGA.



deciding, scheduling and maintaining which hardware resources should be run.

There is no

manage PR regions, i.e.,

facility to



Victor G. Lesau (MASc student) – victor_lesau@sfu.ca *Architecture and design of PR domain, Edward Chen (PhD student) – ekchen@sfu.ca Academic Supervisor: William A. Gruver – gruver@sfu.ca Technical Supervisor: Dorian Sabaz – dorian@iroboticscorp.com Intelligent/Distributed Enterprise Automation Laboratory – <u>www.ensc.sfu.ca/idea</u>

