Architectures and Design Methodologies for Very Low Power and Power Effective A/D Sigma-Delta Converters

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Summary

- Introduction
- Sigma-Delta Architectures
- DAC Resolution Reduction
- Time Interleaved Technique
- OTA Swing Reduction
- Syntesis of the Noise Transfer Function
- Conclusions

Introduction

Technology advancements and the electronics market evolution more and more favor applications with nomadic features:

- Limited power refueling;
- Autonomous operation (no power specifically provided with capability to acquire the power that needs and modulate its activity depending on the available power budget).

Nomadic electronics impose an optimum trade-off between power and performance $\Rightarrow$ Minimum power and its aware use.

Hot Topics

- Ultra-low power analog conditioning;
- Ultra-low power data conversion;
- Power aware digital design;
- Re-design of basic digital cells and power optimization of algorithms.

Introduction (ii)

For the design of data converter an effective use of power is measured by the figure of merit (*FoM*)

$$FoM = \frac{P}{2^{ENOB} \cdot 2 \cdot f_B}$$

ENOB = equivalent number of bits; f_B input bandwidth.

The *FoM* is not a solid way to asses the power effectiveness as it depends on technology and the frequency range of operation.

Nevertheless, obtaining a *FoM* in the range of *1 pJ-conv* or less is a good sign of an effective use of power.

Sigma-Delta Architectures

$\Sigma\Delta$ was for high-resolution, low-bandwidth analog-to-digital converters. Now, $\Sigma\Delta$ is also used for low-power high-bandwidth medium-resolution with small *OSR*.

The low power goal can be obtained by a proper choice of three design parameters: the oversampling ratio, the order of the modulator and the number of bits of the quantization.

- High sampling frequency augments the need of high bandwidth and slew-rate in the used *OTA*s.
- High-order requires a large number of *OTA*s.
- Multi-bit quantizers increases the resolution but multi-bit *DAC*s can cause harmonic distortion.

Design Strategies

Use *DEM* and multi-bit architectures with a maximum number of bits in the *ADC*.

Minimize the number of *OTA*: share functions or use a single op-amp to obtain high order transfer functions.

Reduce the clock frequency by using time interleaving and N-path architectures (+ syntesis of the NTF).

Limit the *OTA* voltage swings for benefiting the slew-rate and using architectures with reduced complexity.

Reduction of the DAC Resolution

A $2^{2.5} \simeq 6$ increases of the number of quantization levels is equivalent to a sampling frequency doubling in a second-order modulator.

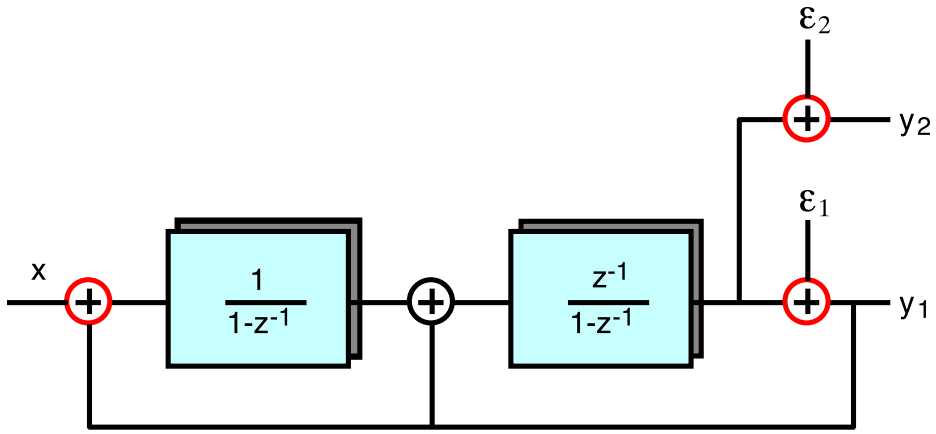
More comparators but lower speed in the op-amps.

Use of Dynamic element matching (*DEM*) of the *DAC* elements.

Solution: use many levels in the ADC but reduces the number of levels of the DAC.

Reduction of the DAC Resolution (ii)

Leslie Sing method is an option ...



$$2^{n_1}\varepsilon_1 = 2^{n_2}\varepsilon_2$$

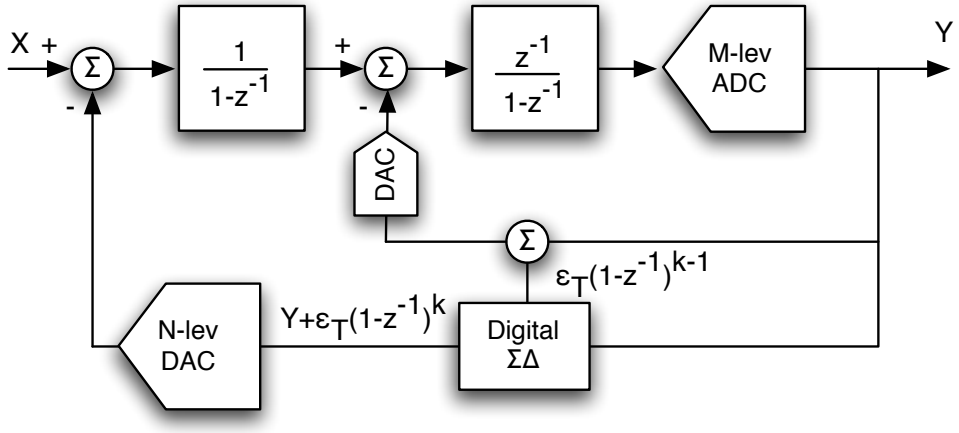
$$y_1 - \varepsilon_1 = y_2 - \varepsilon_2$$

$$y_1 = x \cdot S(z) + \varepsilon_1 \cdot N(z)$$

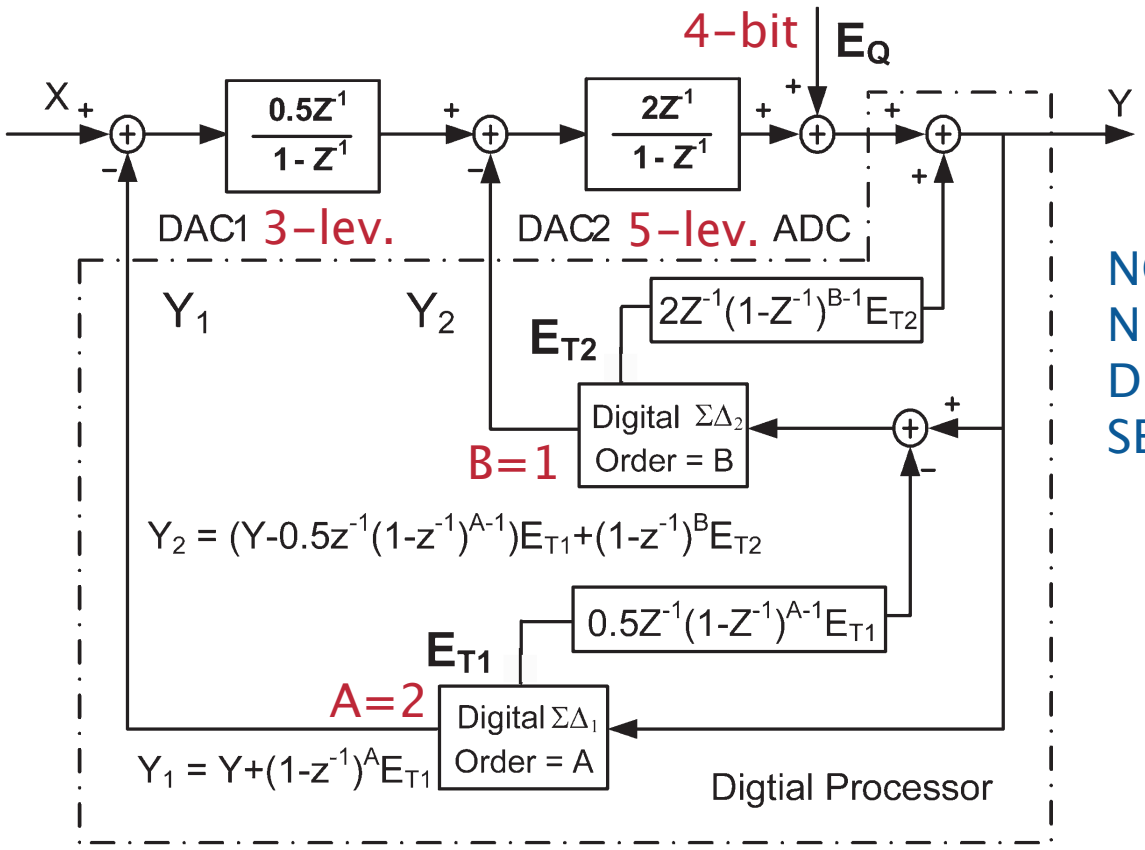
$$y_1 = x \cdot S(z) + N(z)\left[\varepsilon_2 + y_1 - y_2\right]$$

Truncation, Shaping and Error Cancellation

Reduces the DAC resolution by truncation and shaping of the truncation error (Maloberti Yu - JSSC Dec.05).

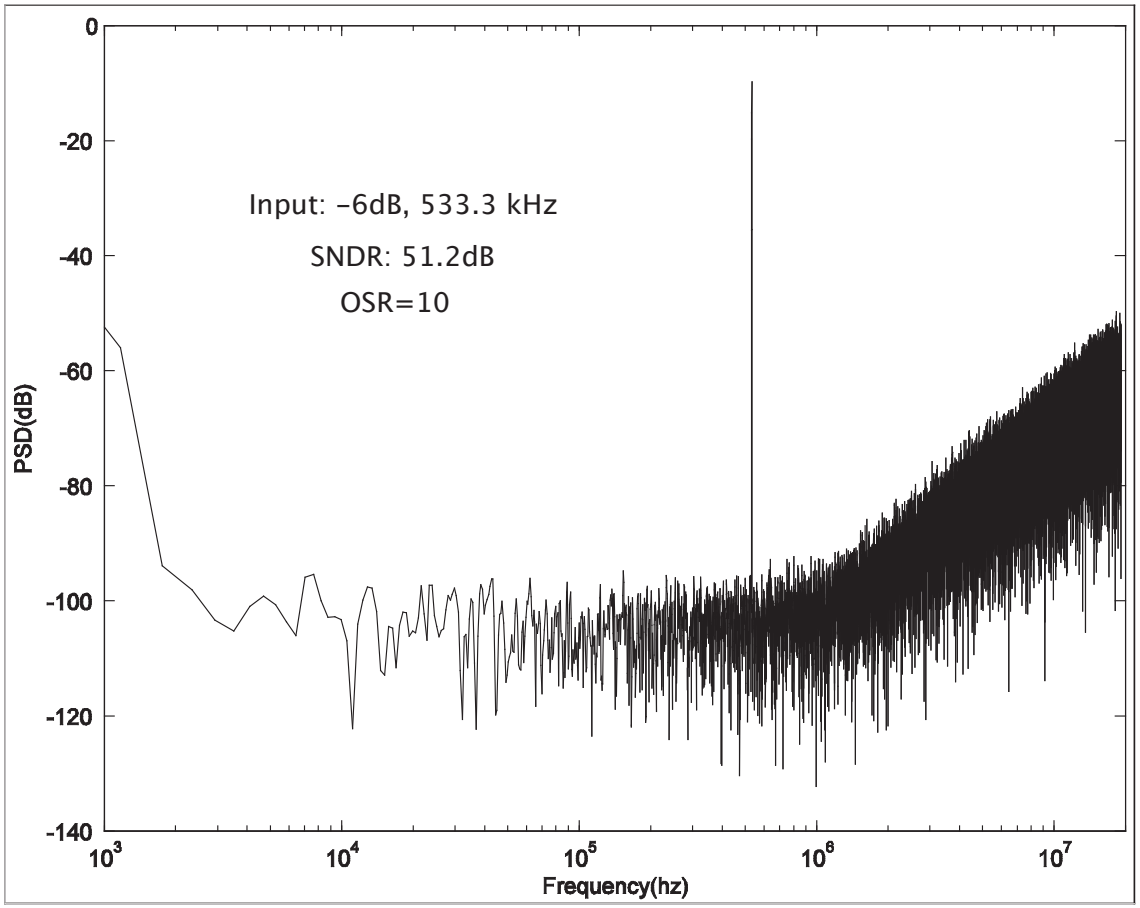


Truncation, Shaping and Error Cancellation (ii)



NO DEMS
NEGLIGIBLE
DIGITAL
SECTION

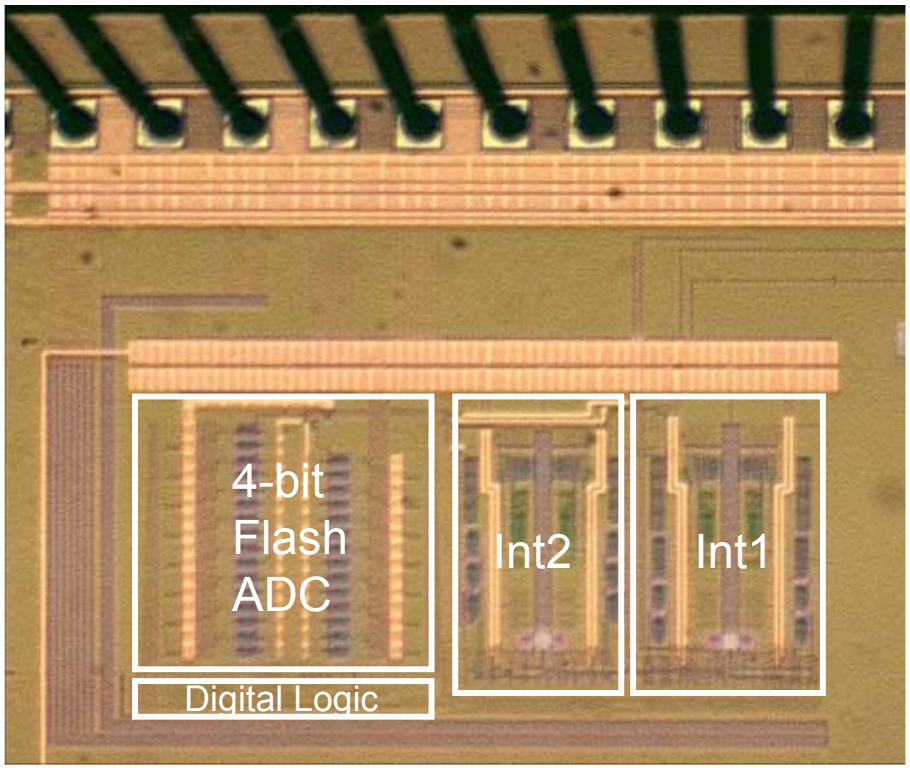
Truncation, Shaping and Error Cancellation (iii)



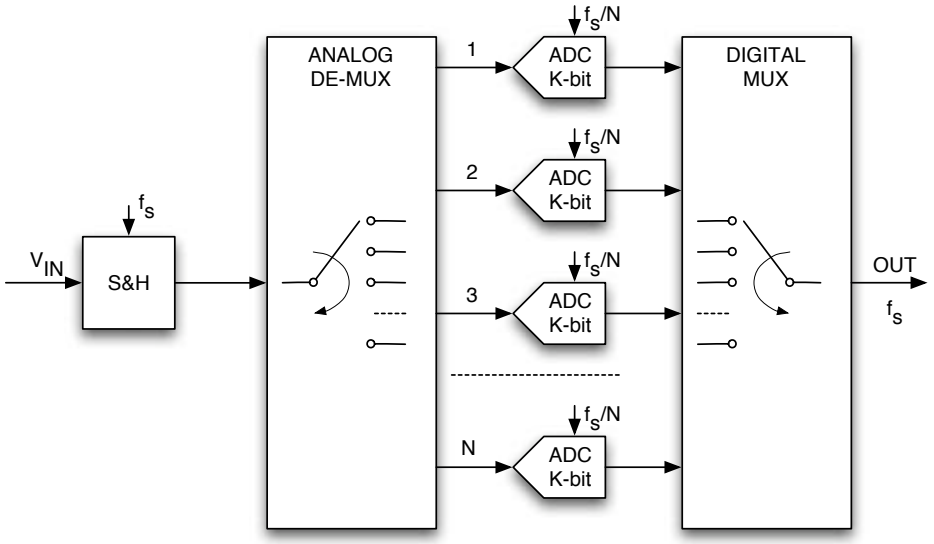
Truncation, Shaping and Error Cancellation (iv)

- CMOS 90nm digital process
- Area: 0.4mm^2
- Digital Part < 5% Layout Area
- Supply 1.2V 2.2 mW
- Signal Band 1 MHz
- OSR=20
- SNDR =64dB

- **FoM =0.92 pJ/conv**



Time Interleaved Technique



Time-interleaved (*TI*) technique ($z \rightarrow z^M$) is attractive for $\Sigma\Delta$ as the *OSR* increases without speeding-up analog blocks.

Reducing by two the clock diminishes power by 3-4 (MOS in saturation)!

Time Interleaved: Key issue

The recursive operation of $\Sigma\Delta$ modulators makes it difficult the transformation of a $\Sigma\Delta$ into its equivalent *TI* structures.

Limitations:

- Quantizer domino (occurs when a certain quantizer output is connected to another quantizer input via an analog block without a delay).

Solution:

△ **Convert to digital incomplete analog inputs.**

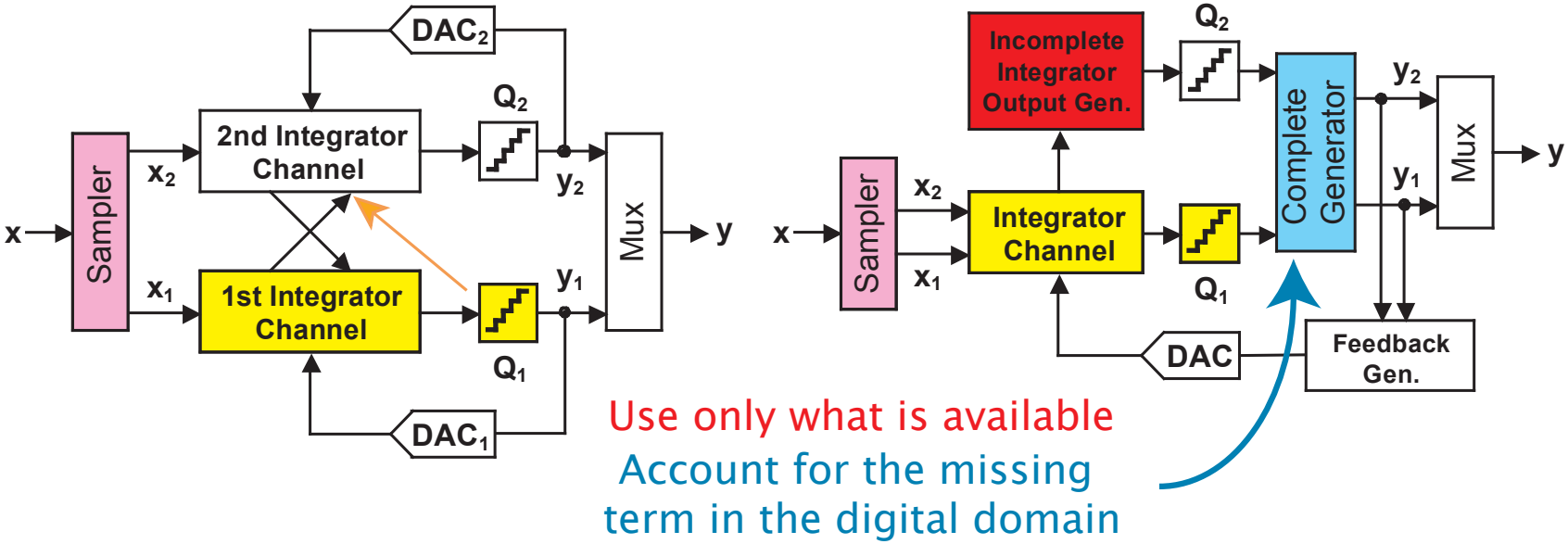
△ **Correct the incomplete result in the digital domain.**

4-paths

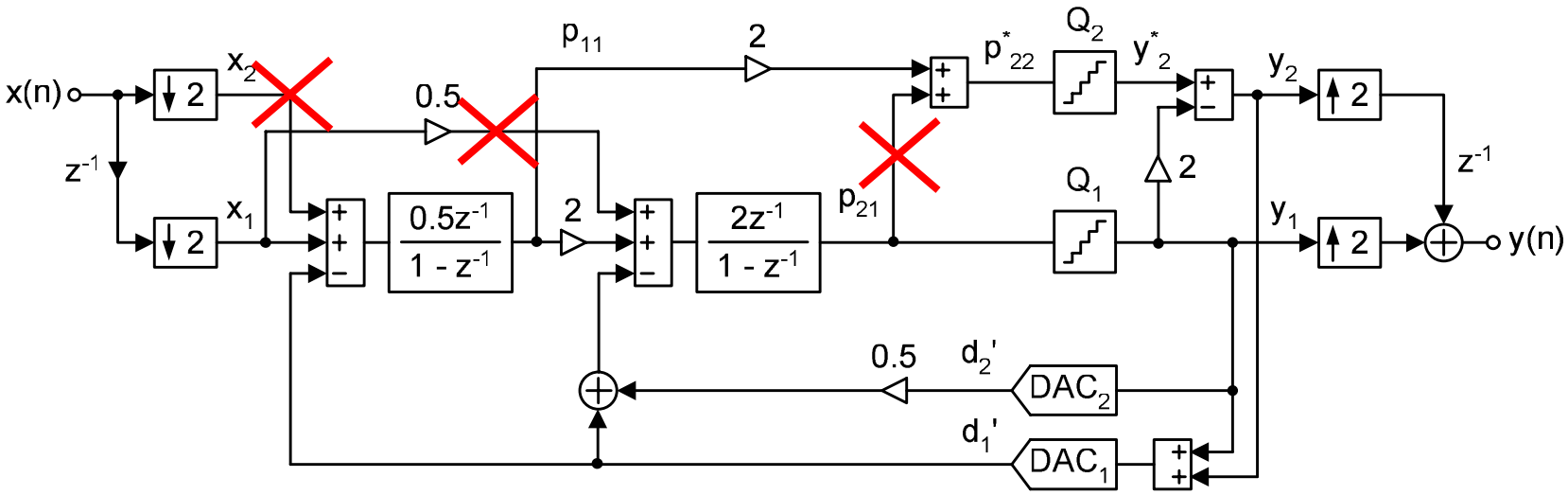
Kye-Shin Lee; F. Maloberti, F. TCAS II 04

Kye-Shin Lee; Sunwoo Kwon, F. Maloberti, F. ISCAS 04

Time Interleaved: Incomplete Conversion



2-path Time Interleaved: Schematic

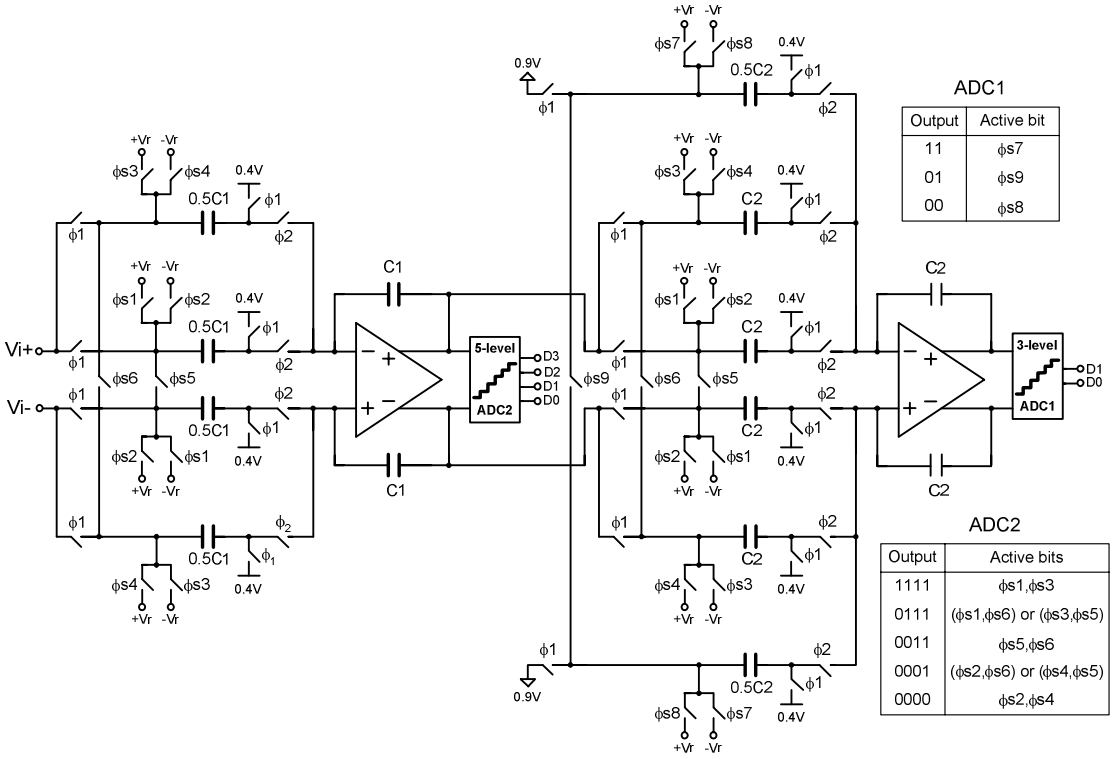


No op-amps for the second path

Use two DACs in the second input

Kye-Shin Lee; Yunyoung Choi, F. Maloberti, ISSCC 06

2-path Time Interleaved: Circuit Schematic



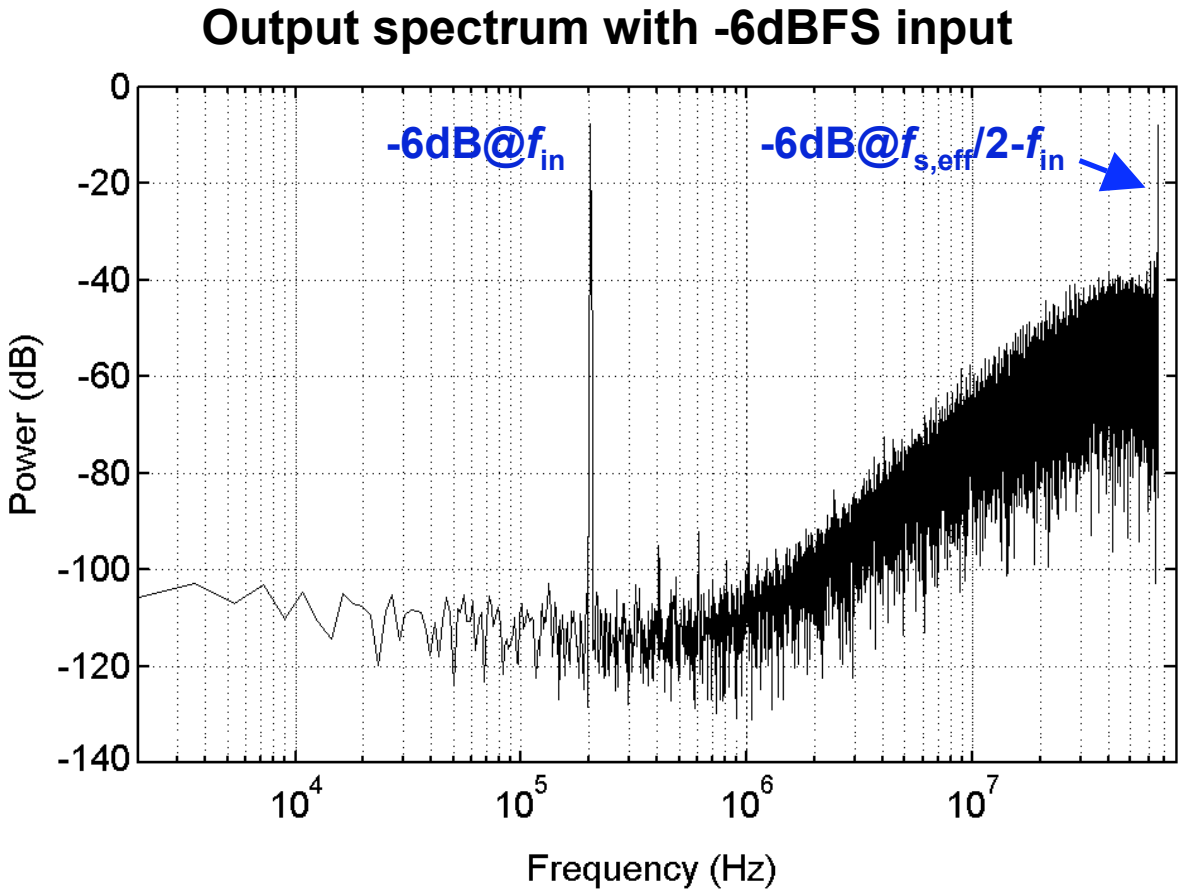
ADC1

Output	Active bit
11	ϕs7
01	ϕs9
00	ϕs8

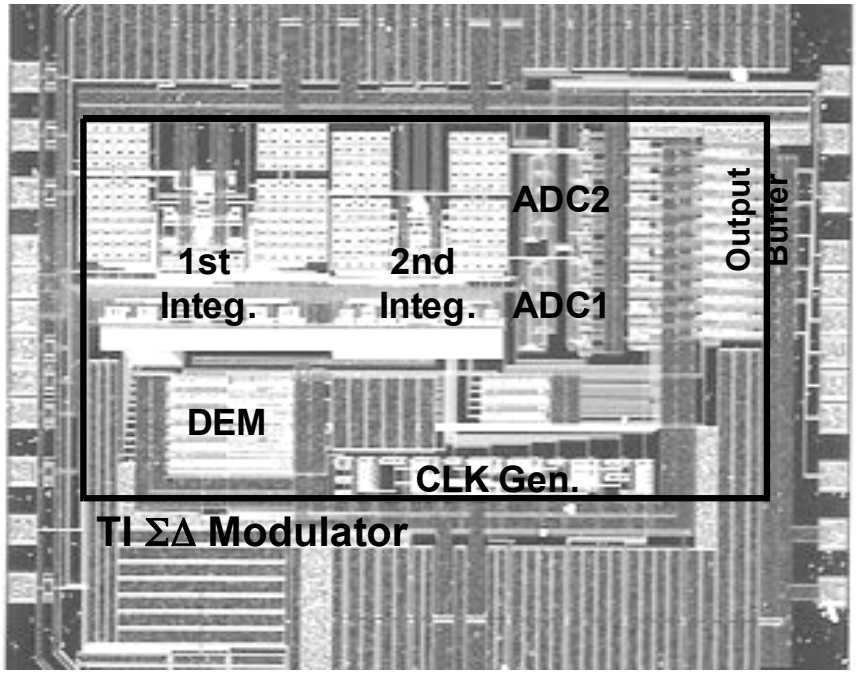
ADC2

Output	Active bits
1111	ϕs1,ϕs3
0111	(ϕs1,ϕs6) or (ϕs3,ϕs5)
0011	ϕs5,ϕs6
0001	(ϕs2,ϕs6) or (ϕs4,ϕs5)
0000	ϕs2,ϕs4

Spectrum of the Output



Chip Micro-photograph



- **Technology**
  0.18um CMOS,
  1-poly / 5-metal,
  MIM Caps.
- **Core Area**
  1.1 mm²

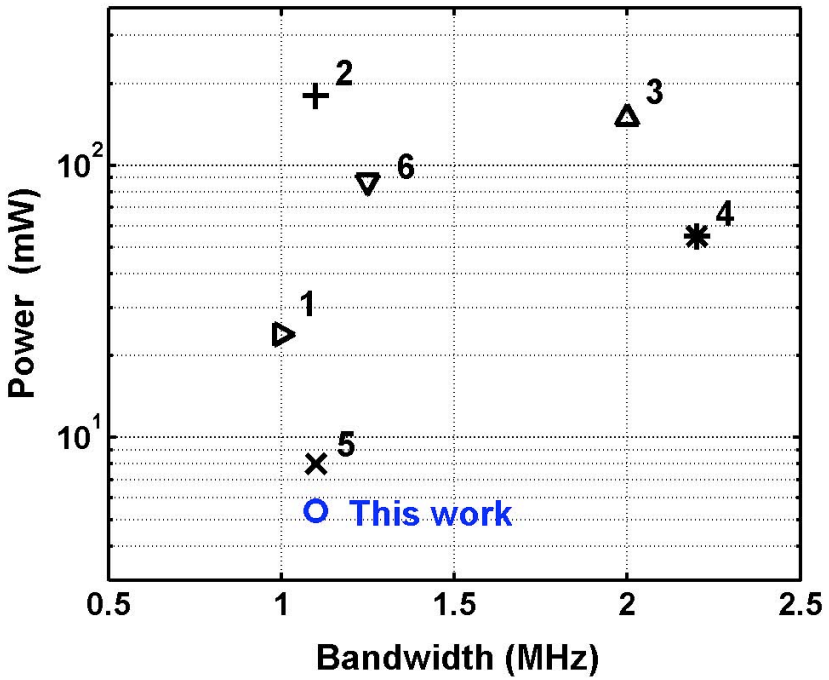
Summary of Performances

Supply voltage	1.8V
Effective sampling frequency	132MHz
Signal bandwidth	1.1MHz
Oversampling ratio	60
Reference voltage	0.8V
Input range (differential)	$1.6V_{pp}$
Peak SNR	81dB
Peak SNDR	78dB
DR	85dB
Power consumption	4.2mW (analog) 1.2mW (digital)
Chip core area	1.1 mm^2
Technology	0.18µm CMOS

FoM = 0.44 pJ/conv

Comparing Results

$$\text{FoM} = \frac{\text{Power}}{2^{(\text{SNDR}-1.76)/6.02} \times 2\text{BW}} \quad [\text{ pJ/con.-level }]$$



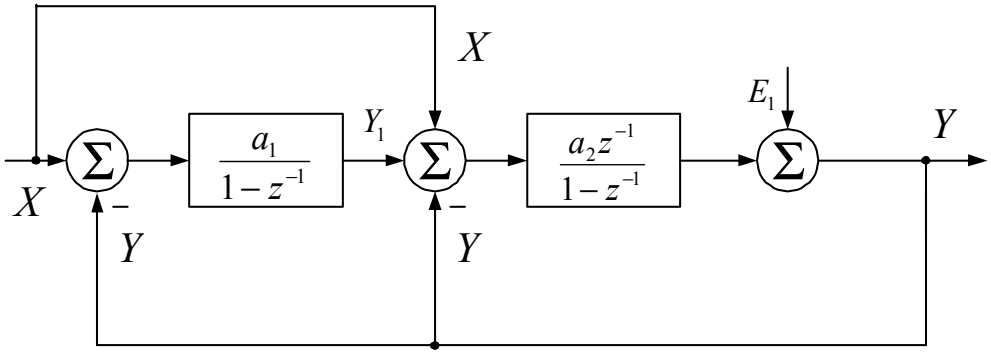
#	ΣΔM	SNDR	FoM
1	Balmelli 2002	79dB	1.65
2	Gupta 2002	88dB	3.87
3	Jiang 2003	82dB	3.62
4	del Rio 2004	73dB	3.42
5	Gaggl 2004	78dB	0.56
6	Nam 2005	89dB	1.34
7	This work	76dB	0.48

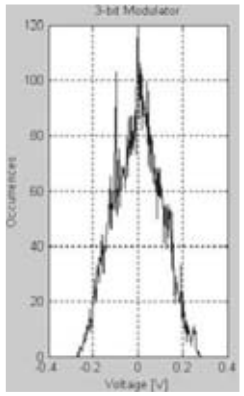
Reduction of the Op-amp Swing

Reducing the output swing minimizes power consumption of the *OTA*:

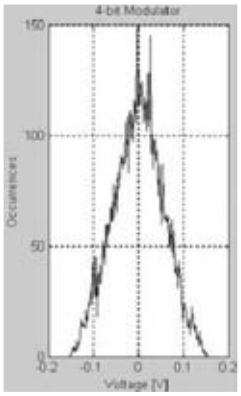
- the slew-rate requirements are relaxed
- the power consumed for charging capacitors is limited
- using power effective *OTA*s like single-stage telescopic schemes

Use of Feedforward





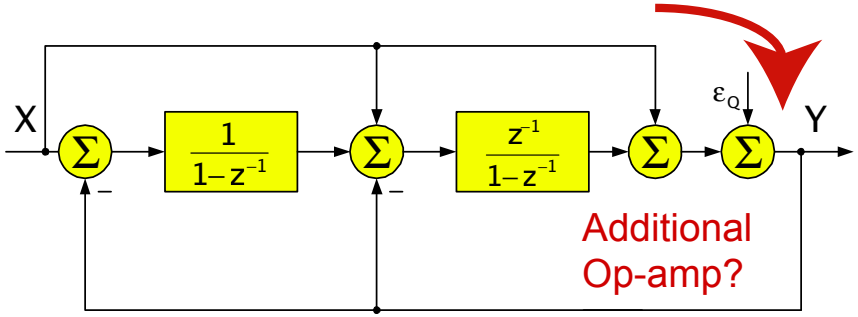
3-bit 0.2 V_FS

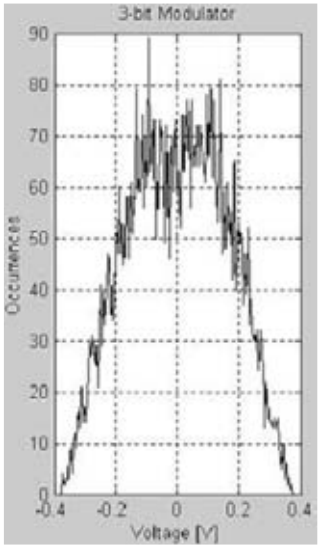


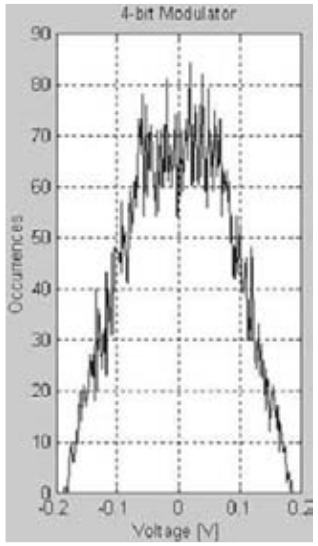
4-bit 0.1 V_FS

The output of the first integrator is almost quantization noise

Use of Feedforward (ii)

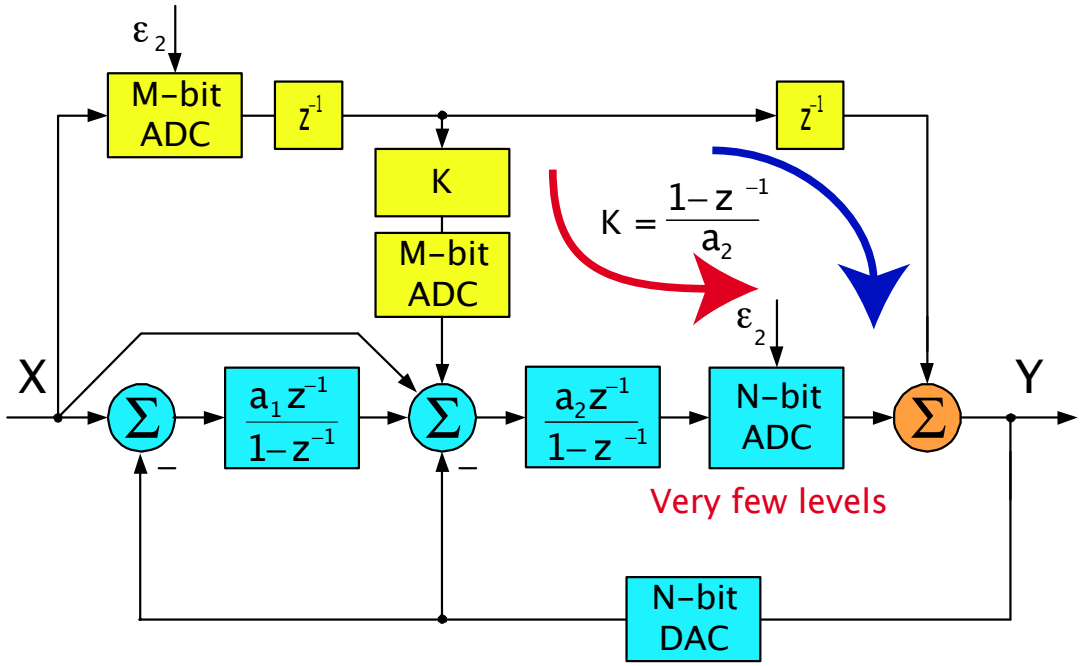






If the feedforward moves after the quantizer .....
The swing at the input of the quantizer is also reduced.
(!) Less levels in the flash required!!

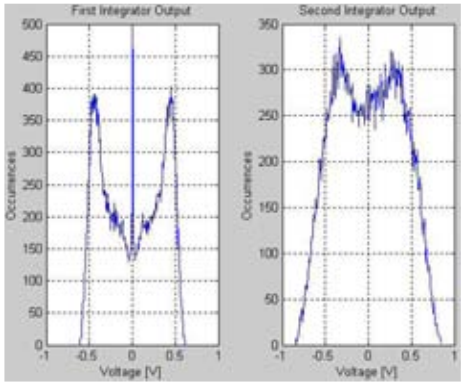
New Solution



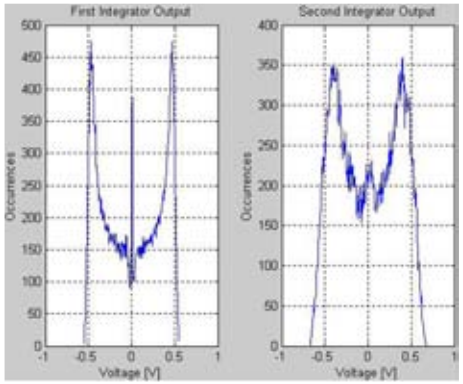
Digital feedforward on the second ”input”

Compensation of the quantization noise with extra path

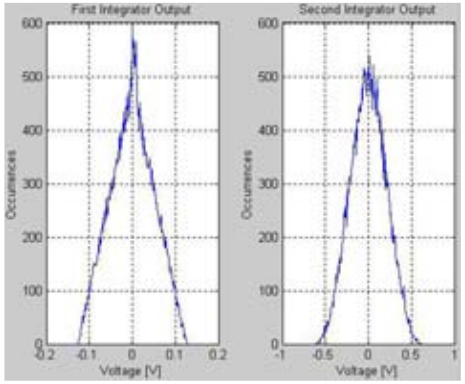
Comparing Solutions



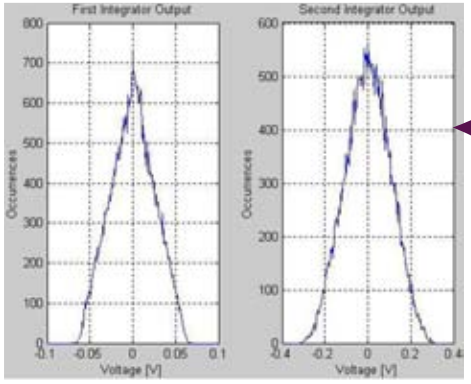
Conventional 3-bit



Conventional 4-bit



3-bit 2-bit feedforward

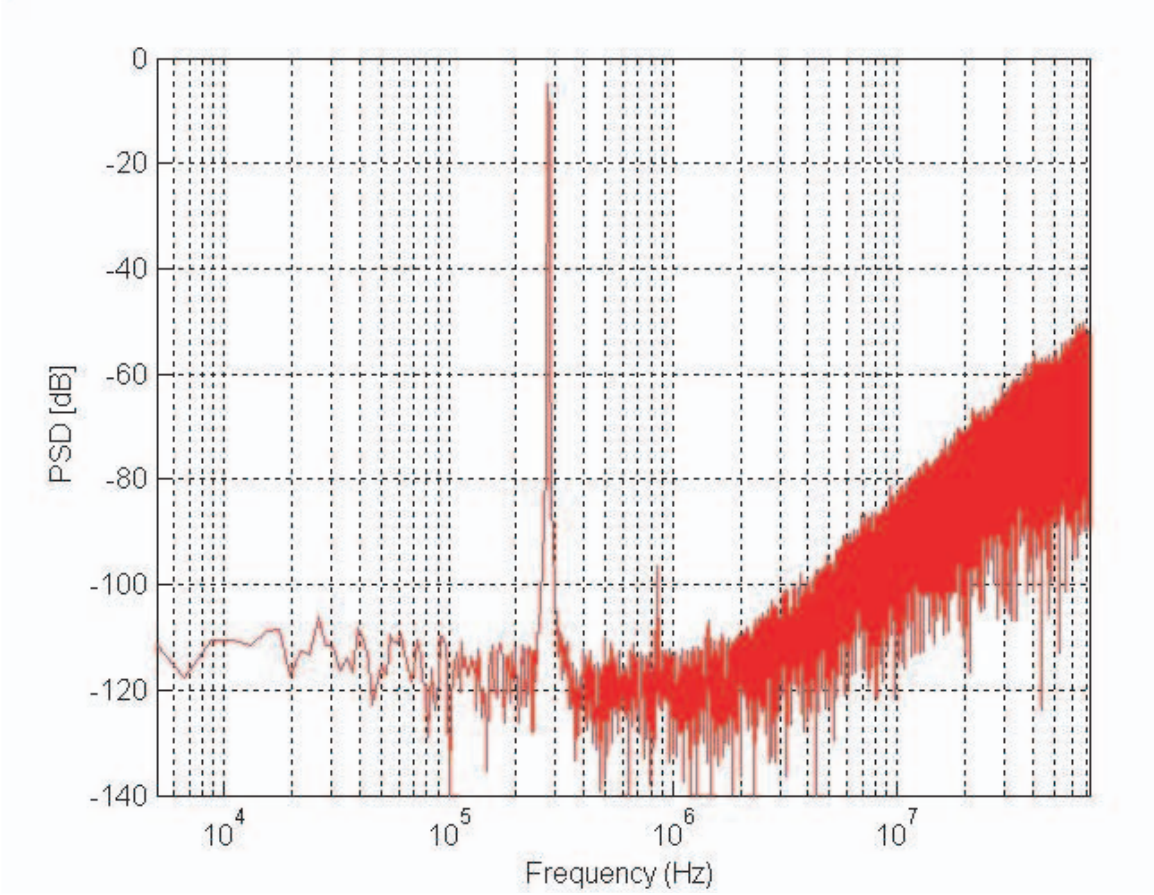


4-bit 3-bit feedforward

7-comparators
5-comparators

Less comparators than the 4-bit (!)

Experimental results



Sunwoo Know, F. Maloberti, F. ISSCC 06

Experimental results (ii)

Sampling frequency	144MHz
Signal bandwidth	2.2MHz
Oversampling ratio	32.7
Peak SNR	84dB
Peak SNDR	79dB
Dynamic range	88dB
Input range	$2V_{pp}$ (differential)
Power consumption	5.1mW (A), 8.7mW(D)
Power supply	1.8V (A), 2.5V(D)
Active area	$2.32mm^2$
Technology	0.18µm CMOS

FoM=0.47 pJ/conv

Syntesis of the NTF

The $z^{-1} \rightarrow z^{-N}$ transformation of an *N*-path scheme increases the order of the *NTF* polynomial. For example, the noise transfer function

$(1 \pm z^{-1})^k$ becomes

$(1 \pm z^{-N})^k$ by using *N*-paths.

Consider a second order modulator and a $z \rightarrow z^2$ transformation

$$NTF' = (1 - z^{-2})^2 = 1 - 2z^{-2} + z^{-4}$$

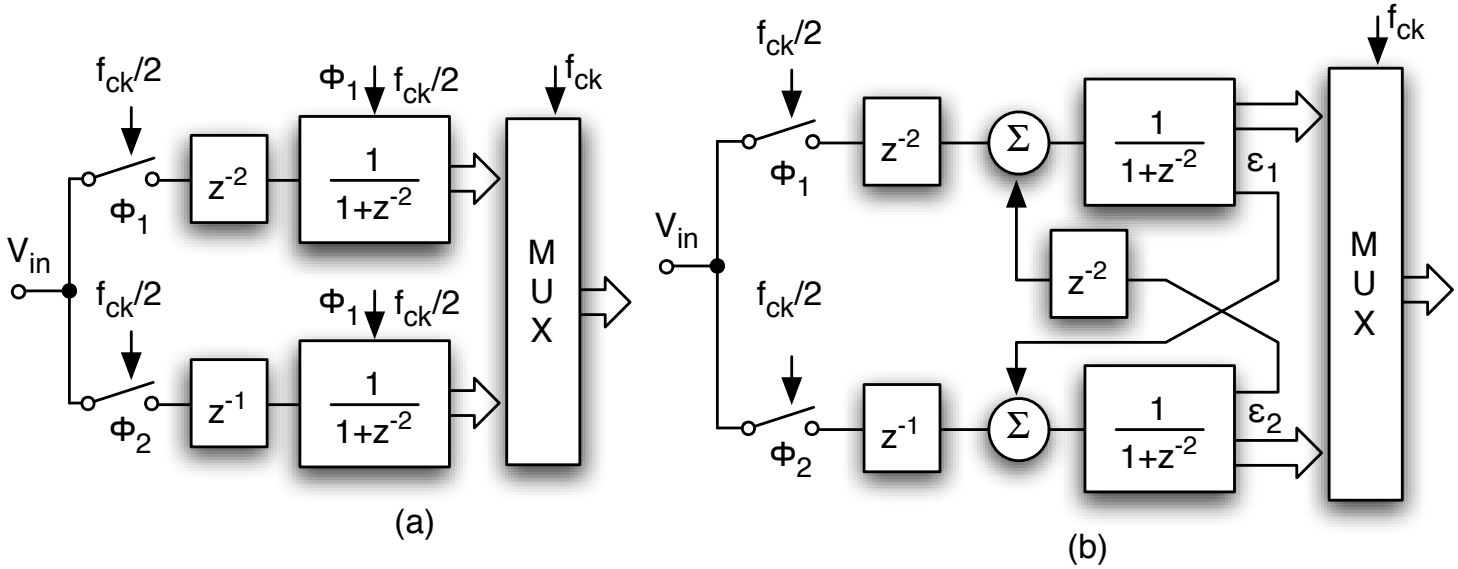
which has the same order as the fourth order noise transfer function:

$$NTF_4 = (1 - z^{-1})^4 = 1 - 4z^{-1} + 6z^{-2} - 4z^{-3} + z^{-4}$$

but is missing the terms $-4z^{-1}$, $8z^{-2}$, and $-4z^{-3}$.

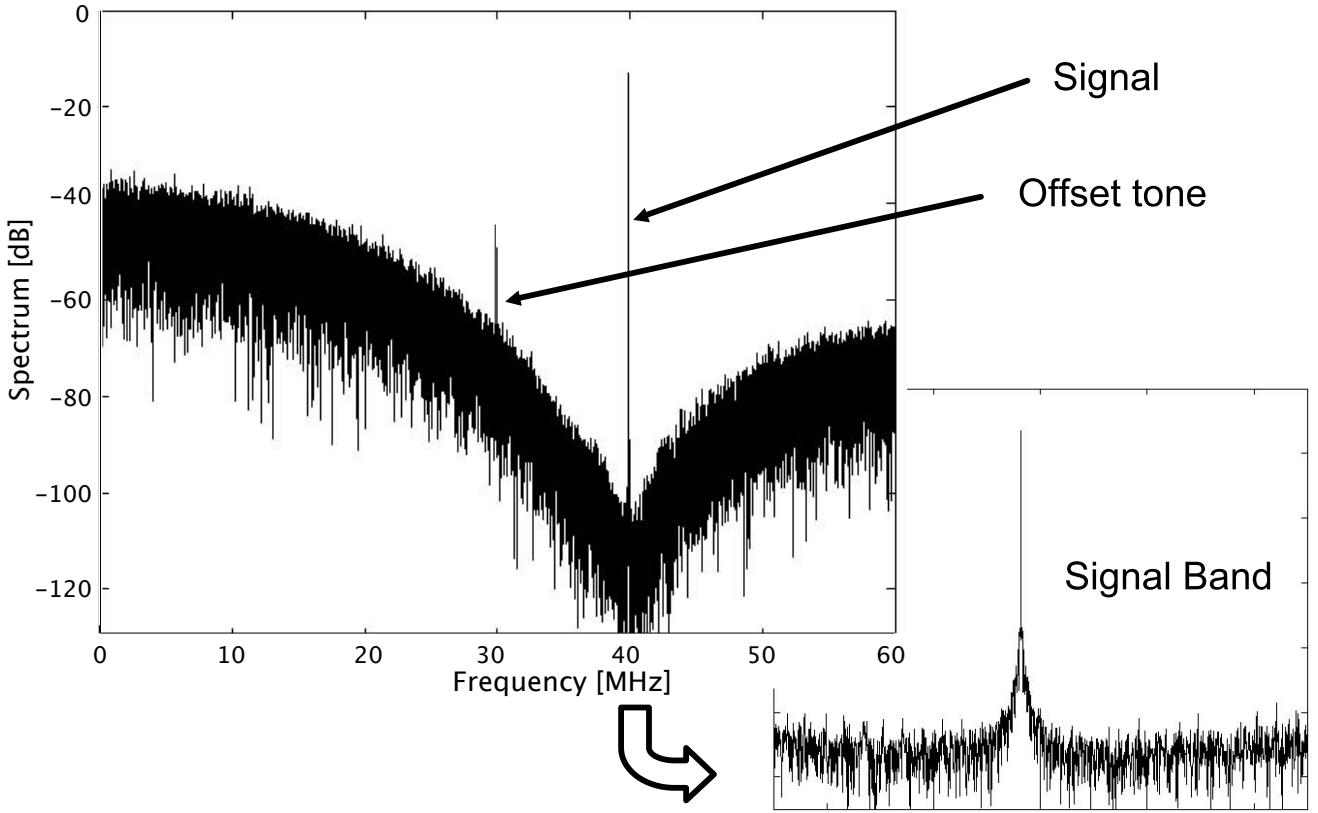
Syntesis means generating the missing terms by suitable additions.

Two-path BP Sigma-Delta



$$NTF = 1 + z^{-1} + z^{-2} \quad \rightarrow (1 + z^{-1} + z^{-2})^3$$

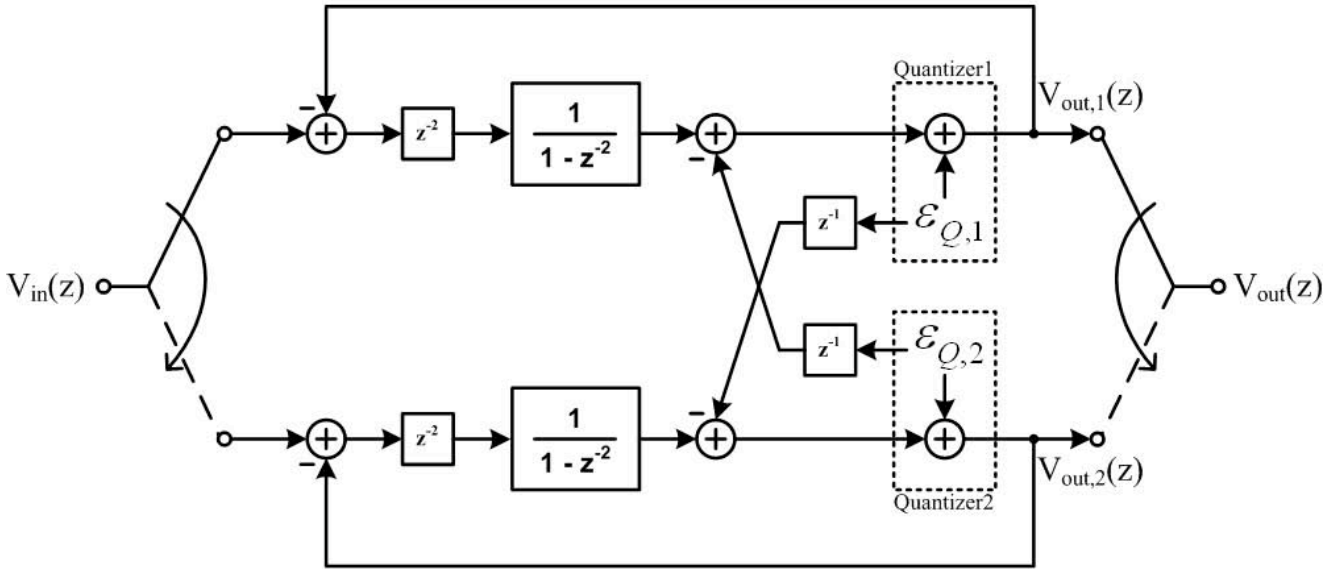
Experimental Results



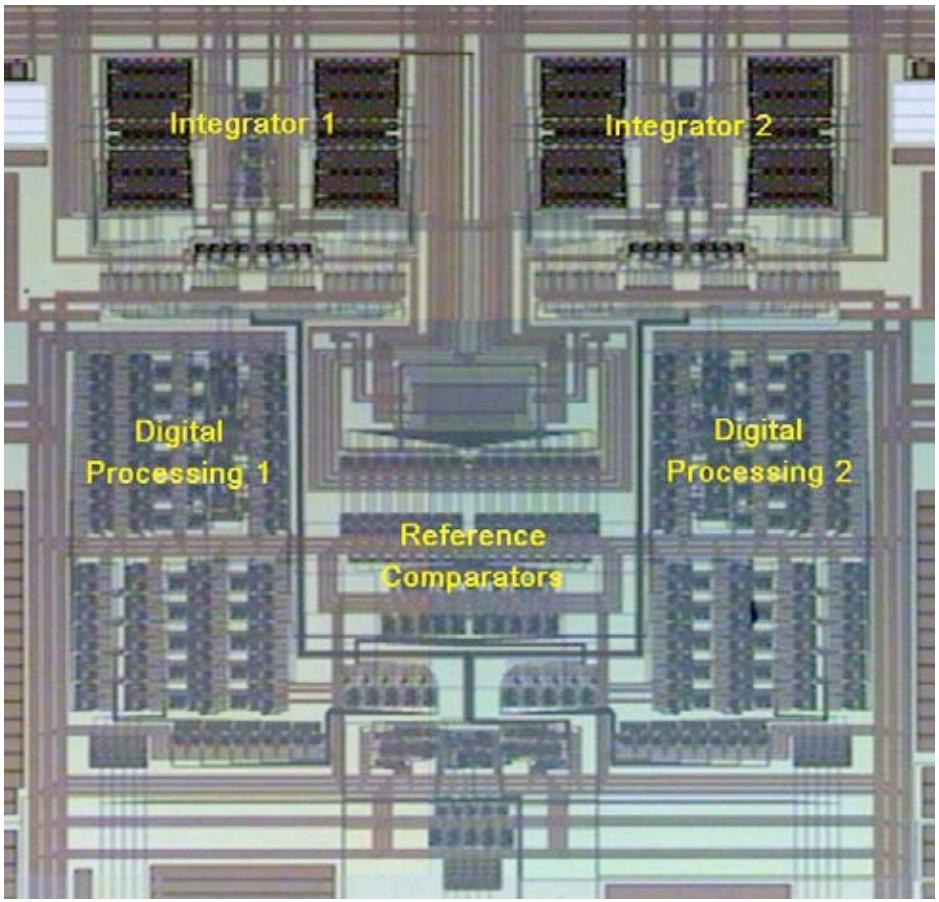
Ying Feng, F. Maloberti, ISSCC 05

Extension of the technique

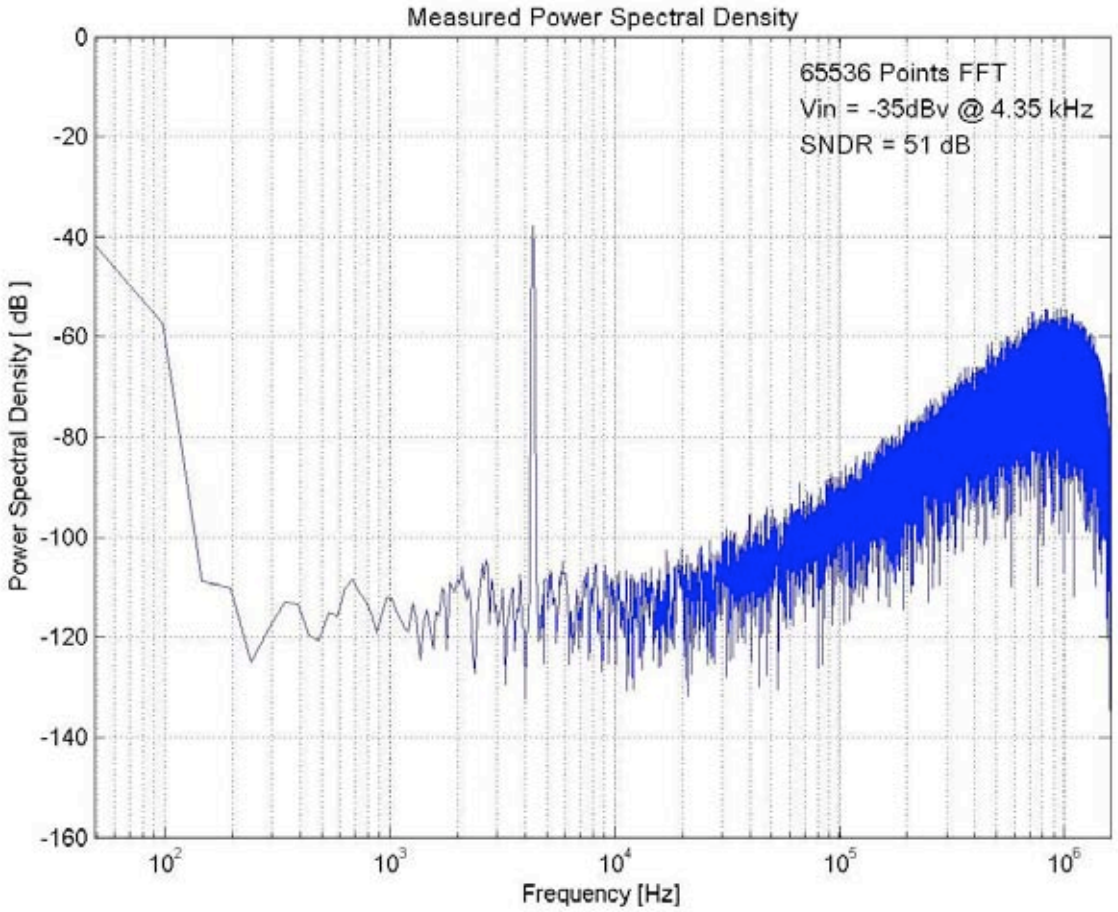
86 dB DR Cross-Coupled Time-Interleaved ΣΔ ADC
for MEMS Microphone with 320 μA Current Consumption



Chip Photo


Integrator 1
Integrator 2
Digital
Processing 1
Digital
Processing 2
Reference
Comparators

Experimental results



Summary of results

MEASUREMENT RESULTS

Sampling Frequency	3.2 MHz
Signal Band	16 kHz
Output Bits	4
Peak SNR	80 dB
SNDR, V_{in} @- 35 dBv	51 dB
Power Consumption	600 µW @1.8V
Dynamic Range	86 dB
Area	1.8 mm × 1.9 mm

Very low current figure of merit!

Conclusions

Data Converters for nomadic systems may need good resolution (SNR) but also ...

Low harmonic distortion

Low, **low low** power and voltage.

Solutions described here determine the following recommendation:
Use digital circuitry for improving analog performances.

THANK YOU!