

Sunshine: A Broadband Packet Switch Architecture

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Outline

- **Requirements**
- **Switch architecture**
- **Performance**
- **Conclusions**

Transport Services

- Circuit Emulation
 - Leased line replacement
 - Setup prerequisite
 - Constant bandwidth ---> Quasi periodic
 - Very low packet loss
- Virtual Circuit
 - Setup prerequisite
 - Small header (VC number)
 - Variable bandwidth
- Datagram
 - No prior notice (setup)
 - Large header (full source and destination)
 - Variable size (up to 10,000 bytes)

Switch Requirements

- **Cell length**
 - 32 --> 128 bytes
- **Transmission rate**
 - 150 Mb/s per line
- **Cell duration**
 - Less than 4 usec (64 byte cell)
- **Module size**
 - Up to 1024 lines

Packet Switch Fabric

- **Batcher/banyan fabric**
 - **Self-routing**
 - **Internally non-blocking**
- **CMOS implementation**
- **3D packaging techniques**

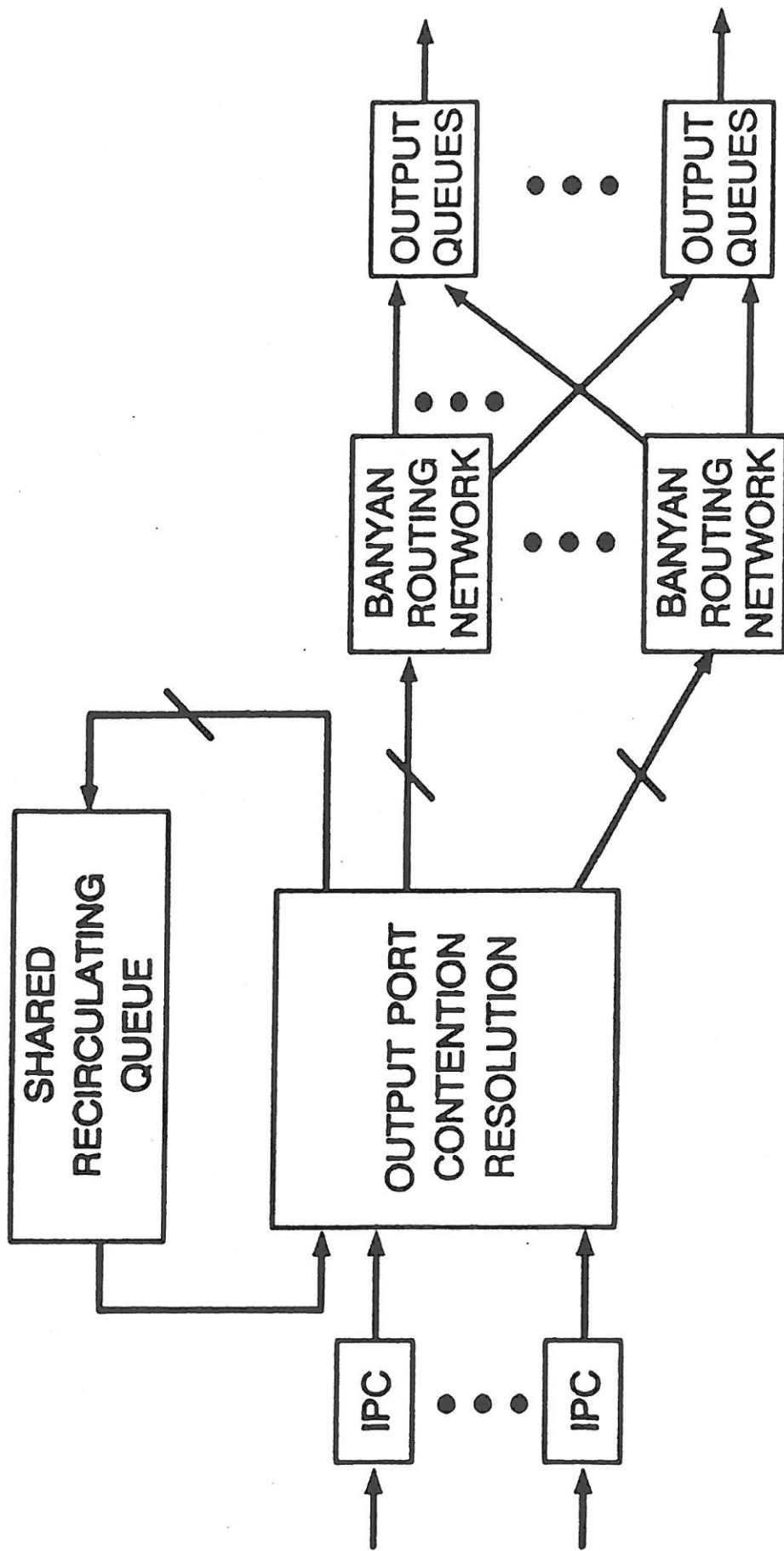
Queuing Alternatives

- Input (3 phase, ring reservation)
- Output (knockout)
- Internal (Starlite, FPN)

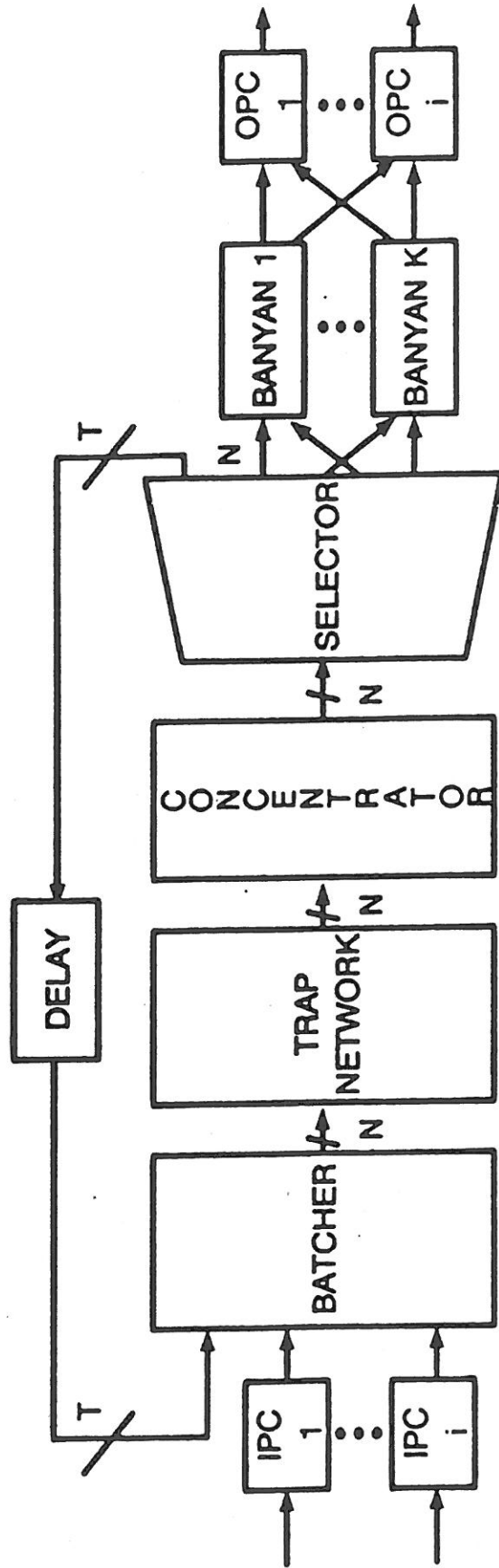
Queuing Strategy

- Multiple locations
- Output buffering (bursty traffic)
 - Sustained batch arrivals
- Recirculation (periodic traffic)
 - Momentary batch arrivals
- Complimentary effects

Conceptual Sunshine Architecture



Sunshine Architecture



Performance

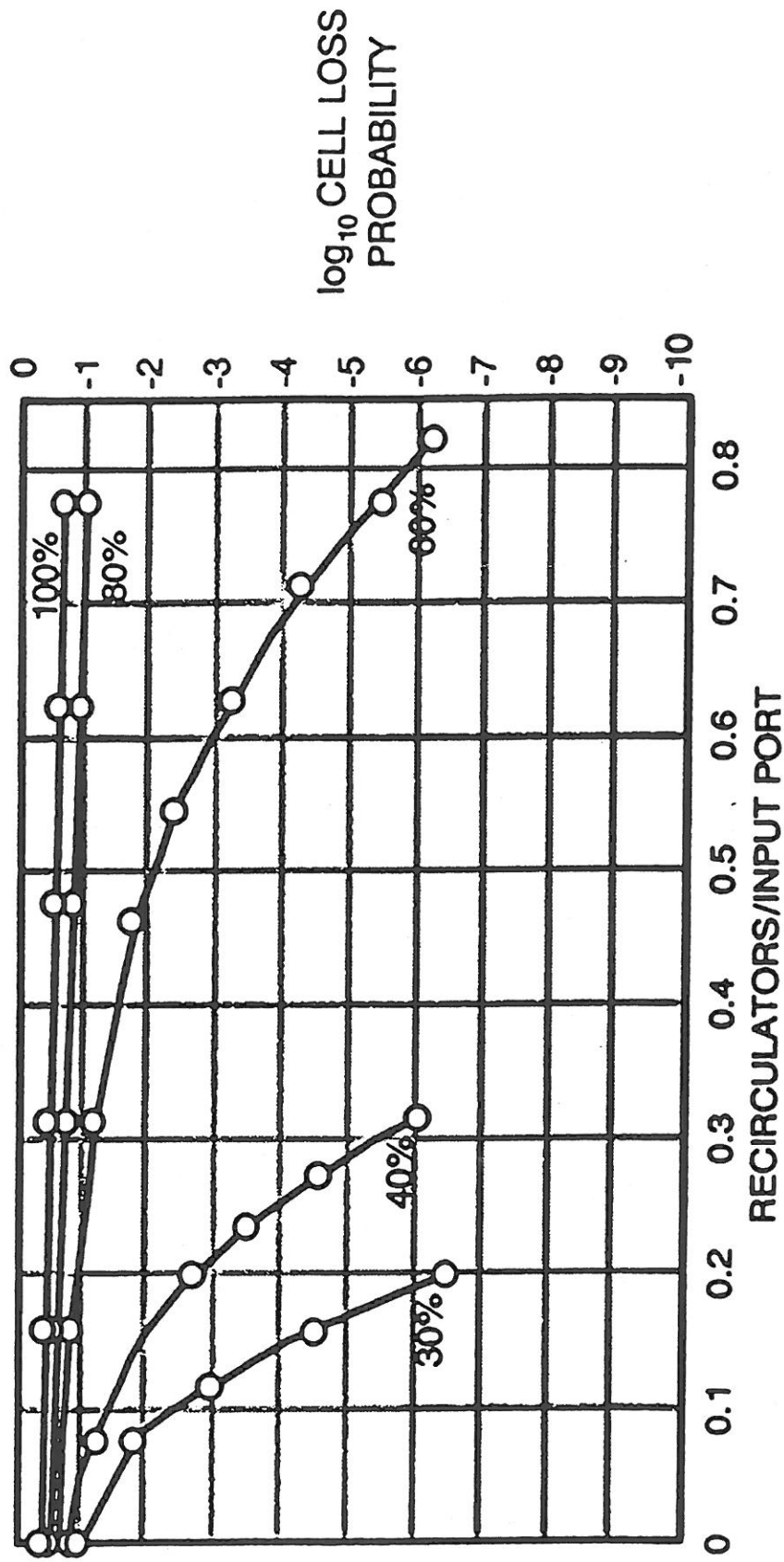
- **Traffic models**
 - **Multiple traffic types**

- **Simulator**
 - **Parallel simulations on 40 workstations**
 - **Small and tailored programs**

Traffic Models

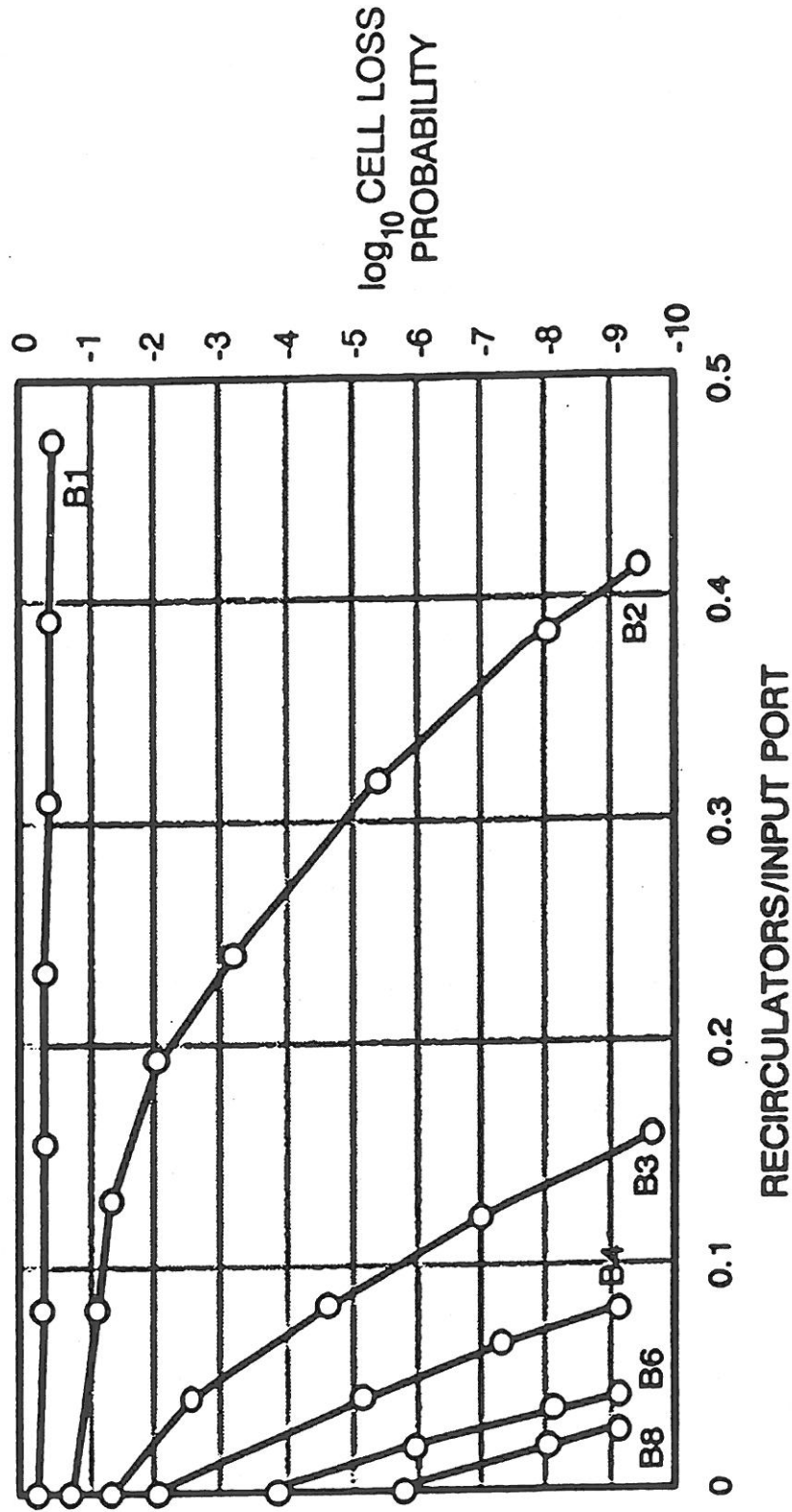
- **Random**
 - Uniform distribution of destination addresses
- **Periodic**
 - Periodic streams interleaved on each input
 - No long term overload
- **Bursty**
 - Long strings of cells from one input to one output

Single Banyan Network



● Random arrivals

Multiple Banyan Networks

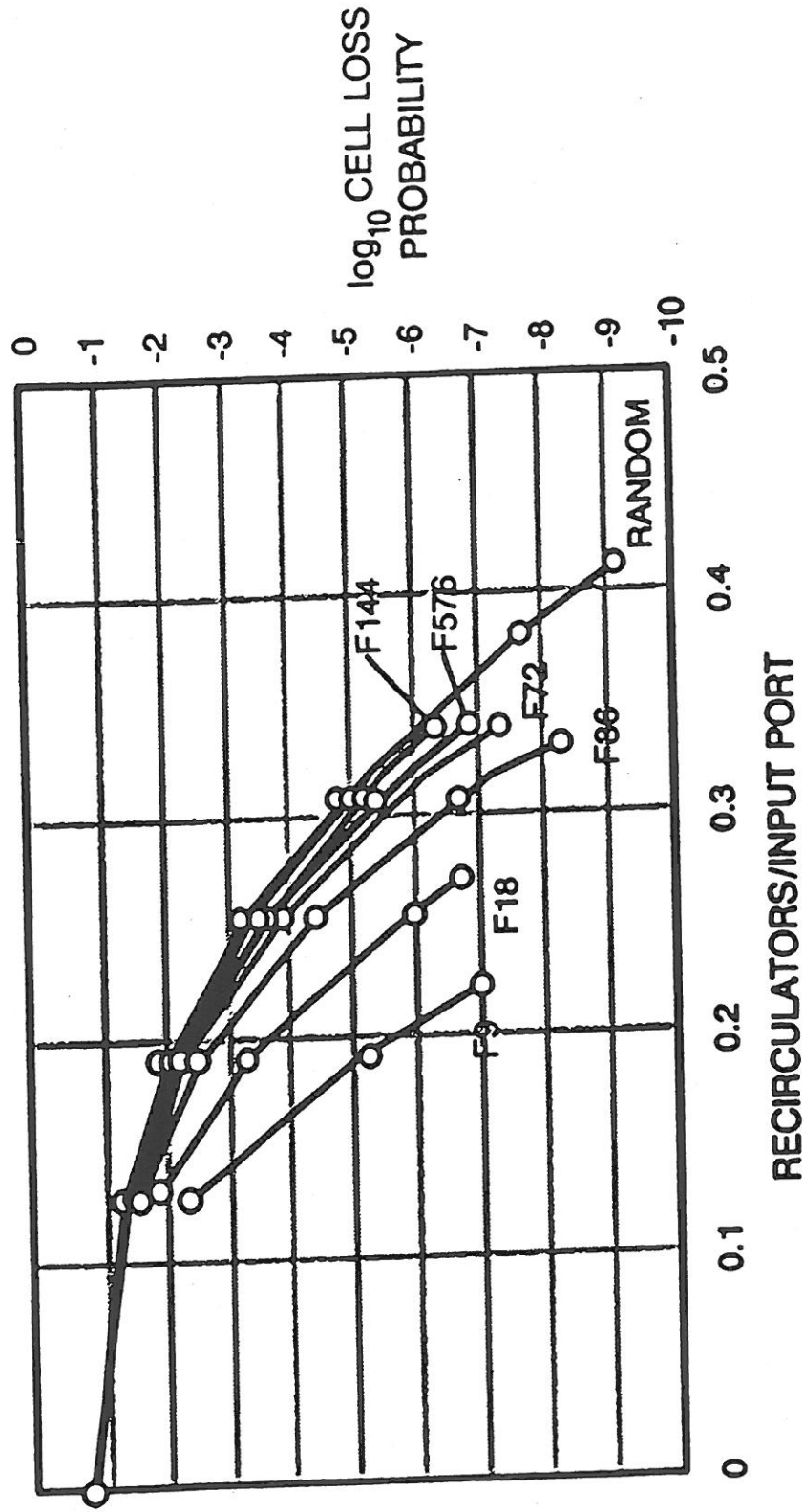


● Random arrivals - saturated load

Periodic Arrivals

- **Concerns**
 - **Blocking patterns**
 - **Low cell loss objectives**
- **Simulation procedure**
 - **Cell pattern repeats every F slots**
 - **Saturated load**
 - **Balanced output loading**

Periodic Performance

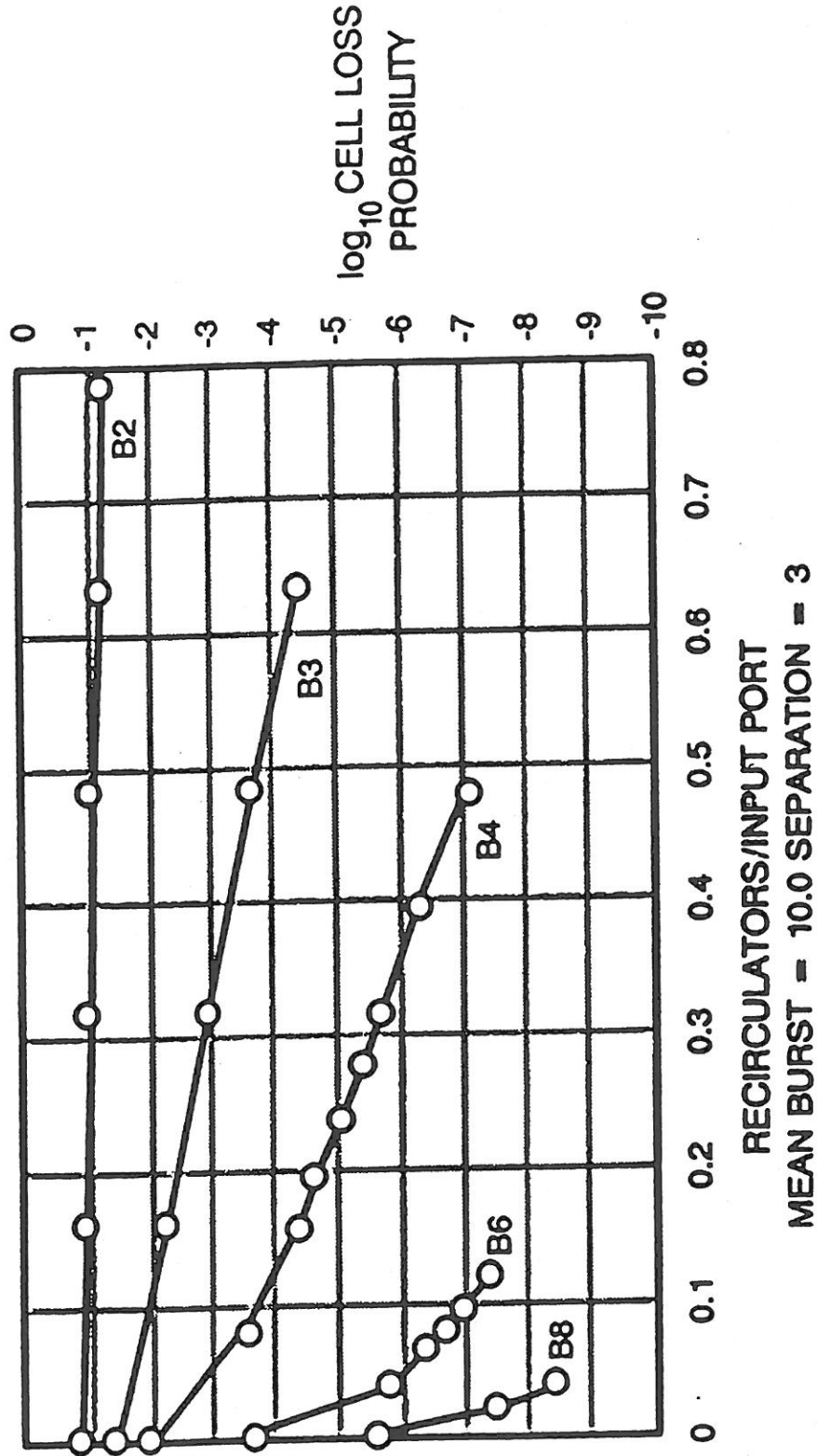


● Saturated load - 2 banyans

Burst Arrivals

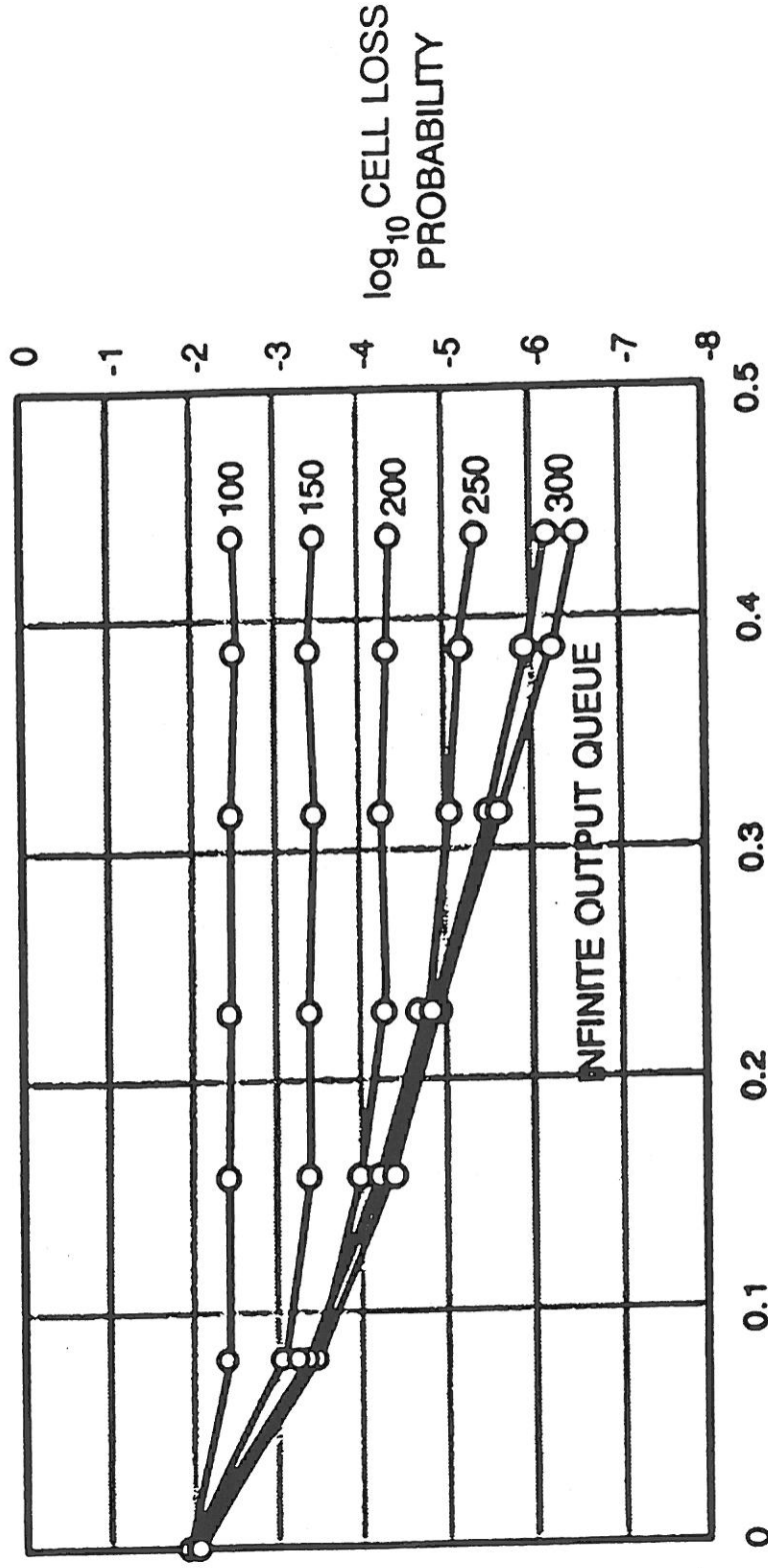
- Critical parameters
 - Burst length
 - Arrival rate (separation)
- Simulation model
 - Geometric distribution

Burst Performance



● Geometric distribution - saturated load

Output Queue Performance



RECIRCULATORS/INPUT PORT
BANYAN = 3 MEAN BURST = 10.0 SEPARATION = 3

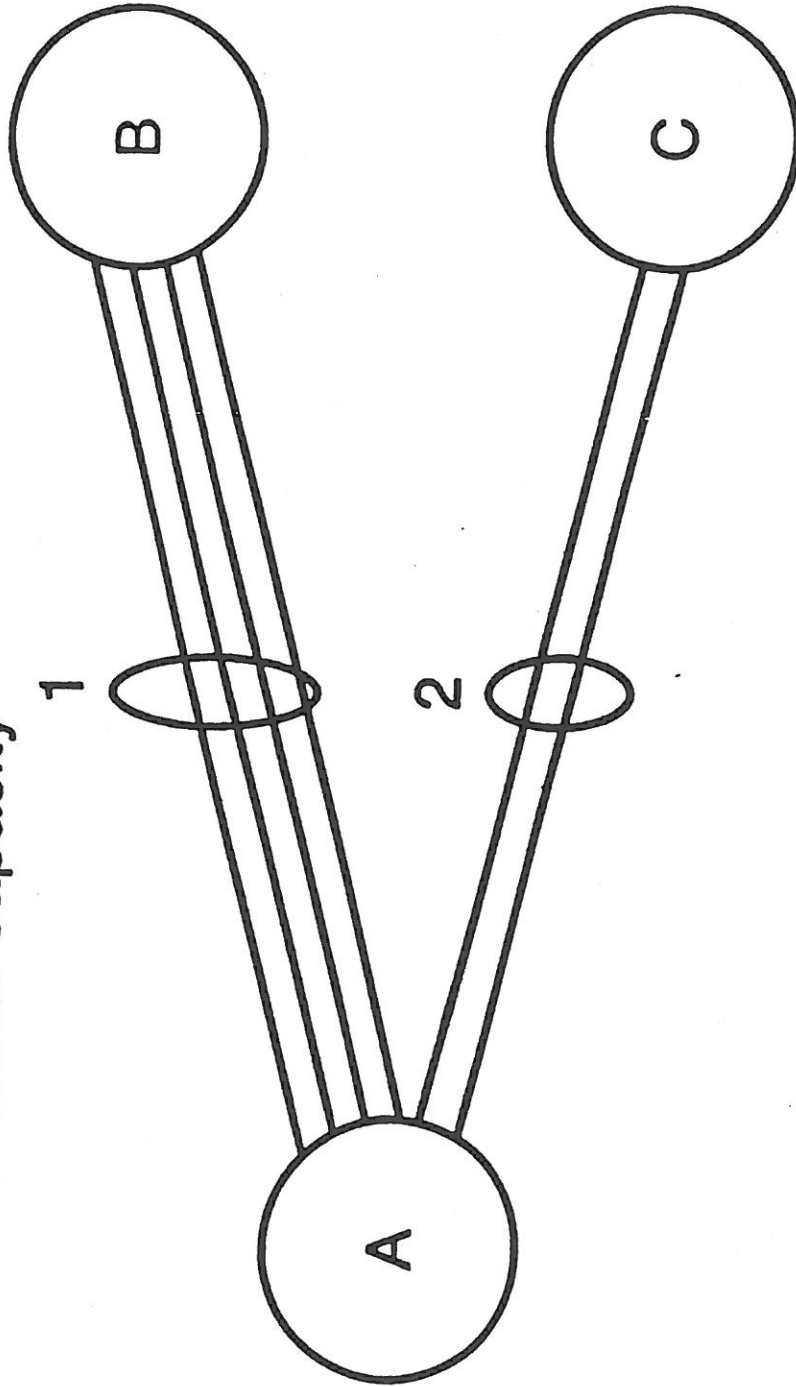
- Geometric distribution - 60% load

Parameters That Improve Bursty Performance

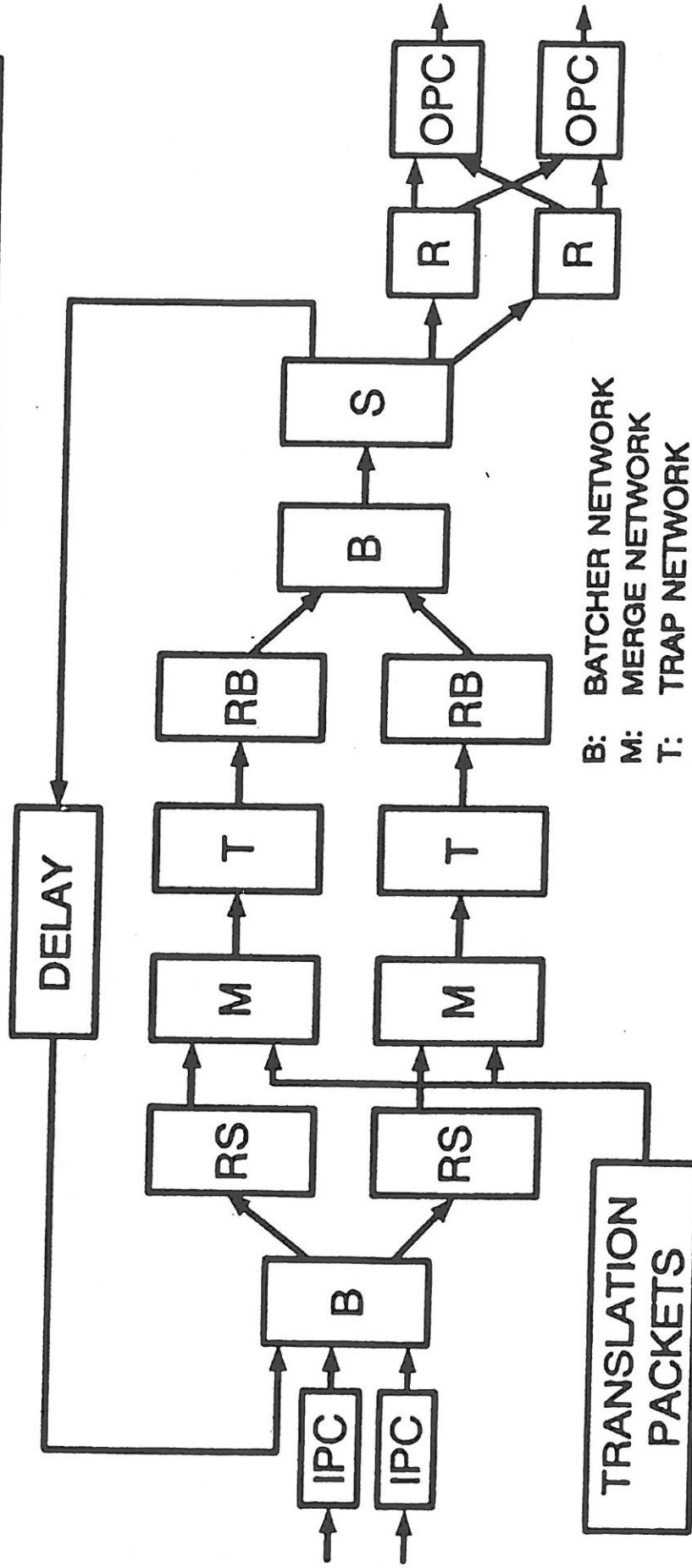
- Reduce access bandwidth
 - Access rate (separation)
 - Link utilization
- Increase channel capacity
 - Trunk groups

Trunk Grouping

- Pool switch resources
- Increased channel capacity



Trunk Group Architecture

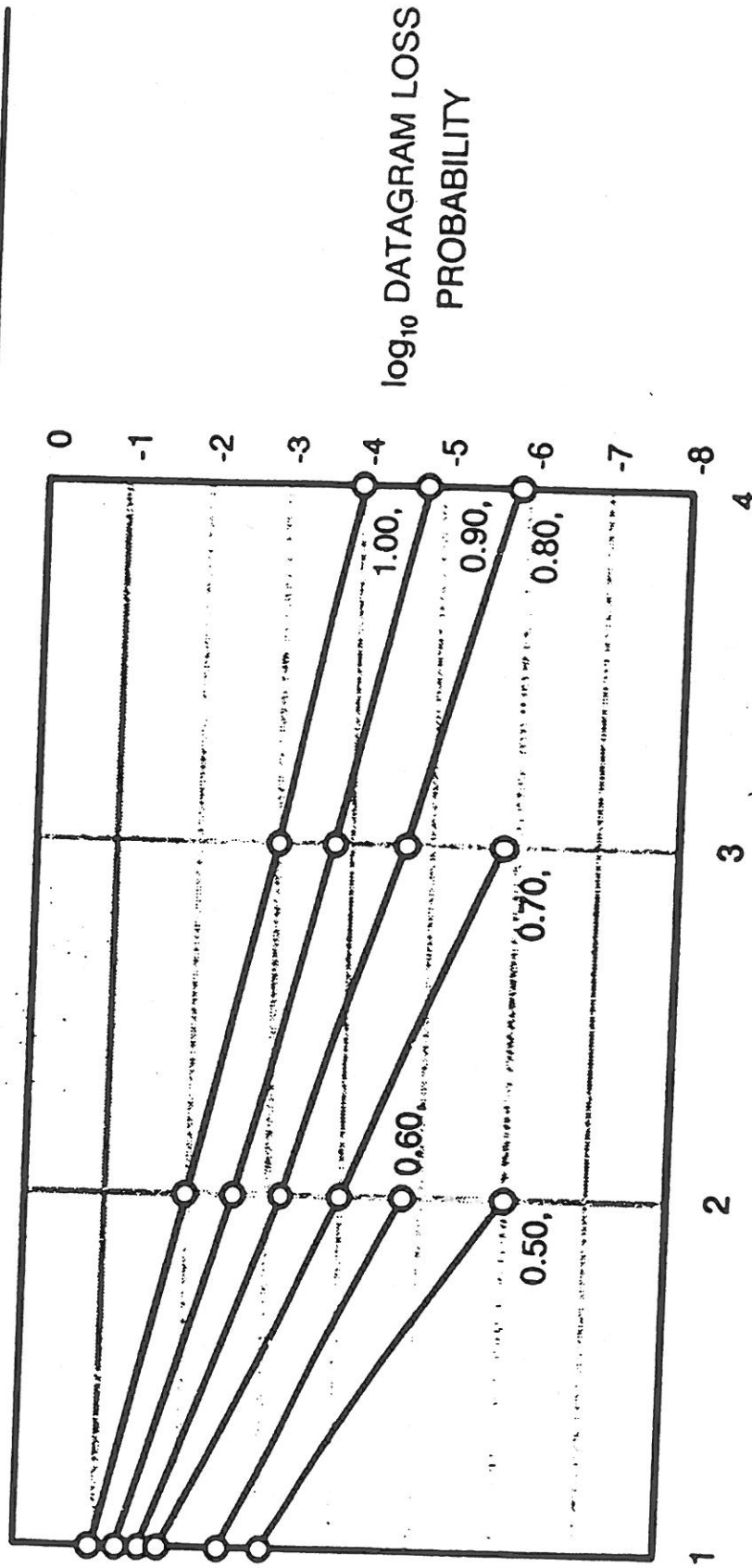


- B: BATCHER NETWORK
- M: MERGE NETWORK
- T: TRAP NETWORK
- RB: REVERSE BANYAN
- S: SELECTOR
- R: BANYAN NETWORK
- RS: RUNNING SUM ADDER

Trunk Group Performance

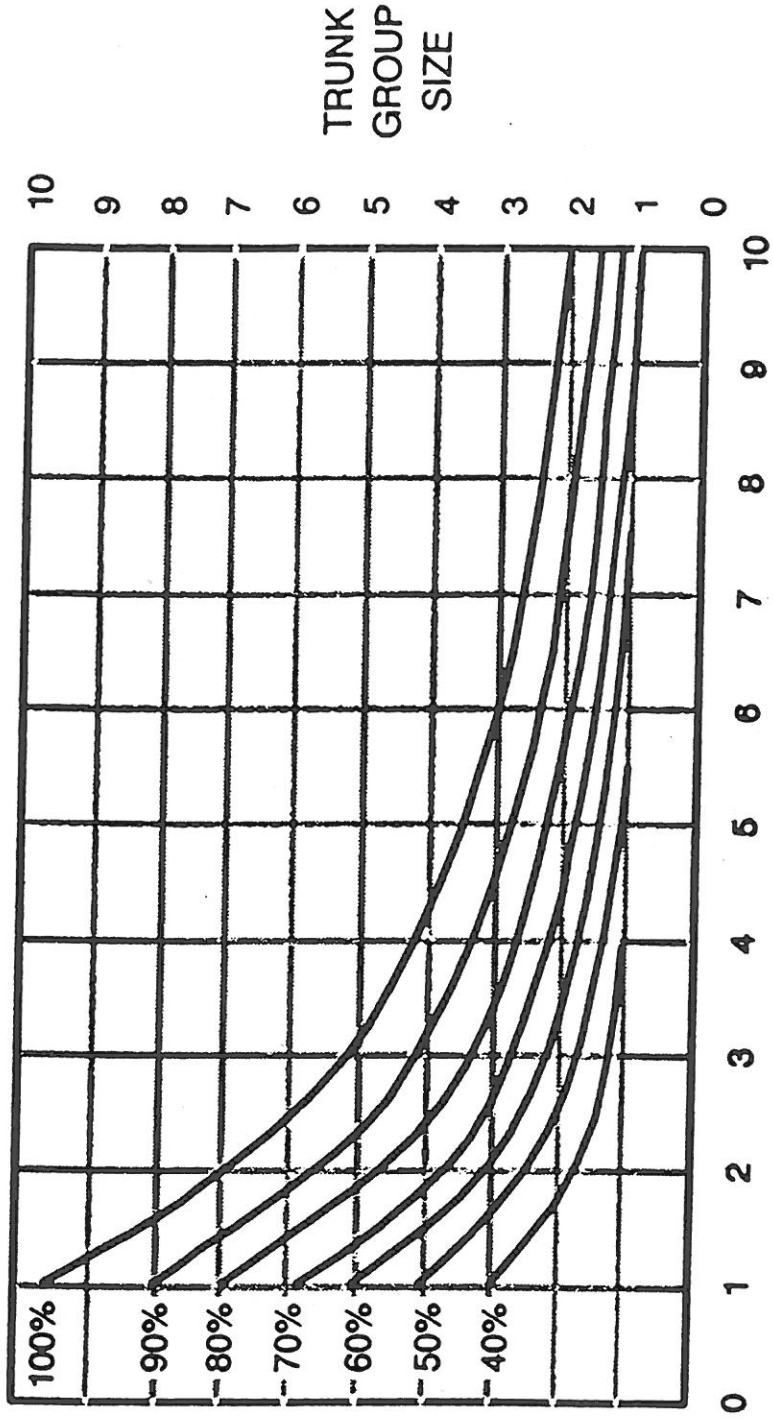
- Datagram distribution (bi-modal)
 - 20% arrivals = 100 cells
 - 80% arrivals = 1 cell
- Switch configuration
 - 0.5 recirculators/input
 - 2 banyans

Datagram Performance With Trunk Grouping



TRUNK GROUP SIZE
CONSTANT INPUT LOADING
BANYANS: 2 RECIRCULATORS/INPUTS: .5 SEPARATION: 3

Trunk Group Sizing



BANYANS = 2 NORMALIZED SHARED QUEUE = .5 CONSTANT DATAGRAM LOSS = 10^{-6}
 SEPARATION

Dynamic Trap Allocation

- Tradeoff link utilization for terminations
- Use idle port controllers as recirculators

Dynamic Trap Architecture

