ENSC 460/895: SPECIAL TOPICS:
THEORY, ANALYSIS, AND SIMULATION
OF NONLINEAR CIRCUITS

CHARACTERIZING MULTIPLE DC OPERATING POINTS OF CIRCUITS USING DIFFERENT SPICE FLAVOURS

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FINAL PROJECT

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Abstract

An investigation into the performance of the numerical engines of four Spice-derived circuit simulators is presented. Spice3f5, HSpice, PSpice, and NGSpice were used to solve for the multiple DC operating points of four circuits known to exhibit such characteristics: the 741 opamp input stage, the opamp feedback circuit with good common mode rejection in BJT and MOSFET implementations, the hybrid voltage reference, and Chua's circuit with nine distinct operating points. The simulators encountered convergence problems during the simulations and well known convergence techniques were employed towards a solution. We have shown that the simulators perform well and the convergence techniques are helpful for the tougher circuits.

1 Introduction

A great number of circuit simulators are available for use by circuit designers. While most of the commercial grade simulators are based off of Berkeley's Spice circuit simulator, they all have been improved to deal with convergence issues and to support additional compact models, to name a few. As the available distributions vary widely in price from free to several thousand dollars, the frugal engineer should ask questions about how the simulators compare, and which will provide best performance versus total cost. This paper discusses an investigation into the performance of the equation solving engines of four selected simulators: Spice3f5, HSpice, PSpice, and NGSpice.

The most difficult part of a circuit simulation is determining the prerequisite DC operating points as problems in convergence may disrupt the simulation. For this reason, this paper will focus on solving for the DC operating points of a collection of four circuits known for their difficulty and convergence issues. First, the simulators and transistor models are characterized in Sections 2 and 3, respectively. The four circuits are presented with their simulation results in Section 4. Next, Section 5 provides a discussion on the results, and conclusions are drawn after that. The appendices include descriptions of the circuits and complete listings of the results.

2 Characterization of Simulators

All of the selected simulators are based on the original Berkeley Spice simulator and so they share many similar features. For example, they all employ a similar syntax to describe circuit connections, use a Newton-Raphson method to numerically solve circuit equations, and provide similar continuation methods when convergence problems arise in simulating difficult circuits. But, since simulators are developed independently, unique features have also been added. Each simulator provides different implementation, optimization, and control of the numerical integration algorithms, which can affect the simulations and so it is important to discuss the differences between each simulator.

2.1 Simulators

In this section, each flavour of Spice used and the features that set them apart are discussed.

2.1.1 Berkeley Spice3f5

The Spice circuit simulator was developed at the Electronics Research Laboratory of the University of California, Berkeley, by Larry Nagel and Donald Paderson [1]. The early version of Spice used a method for nodal analysis which limited the simulator as ideal voltage sources and inductors could not be simulated. Later versions, including Spice3f5, used a modified nodal analysis to avoid these problems. Modified nodal analysis also generates a set of equations that are easier to implement in a computer, resulting in a substantial performance improvement; however, it does also result in a larger system of equations. Table 1 compares the required steps for both the standard nodal analysis and the modified nodal analysis for a system of n nodes and m voltage sources.

Table 1: Comparison of Nodal Analysis Methods

Standard Nodal Analysis [2]	*Modified Nodal Analysis* [3]
1. Select a reference node (ground). 2. Name the remaining *n-1* nodes and label a current through each passive element and each current source. 3. Apply Kirchoff's current law to each node not connected to a voltage source. 4. Solve the resultant system of *n-1-m* unknowns voltages.	1. Select a reference node (ground). 2. Name the remaining *n-1* nodes and label a current through each current source. 3. Assign a name to the current through each voltage source. 4. Apply Kirchoff's current law to each node. 5. Write a voltage equation for each voltage source. 6. Solve the system of *n*-1 voltages.

Spice3f5 also provides a handful of pre-packaged compact models for devices like MOSFETs, BJTs, diodes, capacitors, resistors, and transmission lines; however, only a limited number of models are supported and the only way to include further compact models is to directly modify the source code and recompile the simulator. This is a result of lack of further development to Berkeley Spice owing to the restrictive license it is released with.

2.1.2 HSpice

HSpice is widely considered within the engineering industry as one of the top commercial circuit simulation packages available, offering a range of features and simulation support for RF, IC, and signal integrity analysis. It also boasts a well developed GUI and an ability to simulate up to 100,000 transistors simultaneously.

HSpice also provides a number of `.OPTION` statements for control and optimization of the numerical computation algorithms. Of particular interest to this investigation are those that control the convergence and accuracy of the numerical solvers. The options unique to HSpice are listed in Table 2.

Table 2: HSpice Unique Options

Option	*Description*
CONVERGE	Invokes different convergence techniques
DCFOR0	Sets the number of iterations calculated after convergence in the steady state
DCHOLD	Specifies the number of iterations to hold nodes at .NODESET
DCSTEP	Convert DC model and element capacitors to a conductance to enhance DC convergence properties
DV	Max iteration to iteration voltage change for all circuit nodes in DC and transient analysis
GMAX	Conductance in parallel with current sources used for .IC and .NODESET statements
GMINDC	Conductance in parallel with pn junctions and all MOSFET nodes, use for DC analysis
GRAMP	Conductance range over which GRAMP is swept
GSHUNT	Conductance added from each node to ground
NEWTOL	Calculates one more iteration past convergence for every DC solution and time point circuit solution calculated

Like Spice, HSpice is also pre-packaged with a number of compact models for fundamental devices, and for each device there are a number of models of varying complexity. The more sophisticated models are MOSFET models, owing to the fact that the majority of IC applications use MOSFET rather than BJT devices. Plus, more models can be readily included into HSpice so that new or custom devices can be supported.

2.1.3 PSpice

As opposed to some other Spice flavours, PSpice provides a wide-ranging GUI environment for simulating circuits containing analog devices. Circuit designs can be captured schematically using the extensive model libraries. The capture ability converts the schematic into the familiar Spice text-based circuit descriptions, which could be edited by the user if so desired. Built-in GUI modules for editing stimuli and viewing output waveforms are also included. Because of its GUI ability, PSpice is a leading simulator standard for the MS Windows platform.

In general, however, PSpice has a weaker numerical engine than the other three simulators in this study. Convergence issues are more rampant with PSpice and greater numbers of convergence iterations are to be expected. The kinds of analyses which can be performed in PSpice are also limited. For this study, a student license for PSpice was used, restricting all simulated circuits to a maximum of ten transistors. Hence, only two of the four circuits (the hybrid voltage reference and Chua's nine distinct operating point circuits) could be tested.

2.1.4 NGSpice

NGSpice is a new open source simulator based on Spice, Cider, and Xspice; it seeks to become a full-feature mixed-level/mixed-signal circuit simulator. Currently this package is still in an early stage of development but as NGSpice is based on pre-existing code it already has a sufficient functionality for inclusion in this study. As well, its developers claim to have improved upon the original Berkeley Spice through bug fixes, improvements to the numerical computation algorithms, and the inclusion of newer compact models.

Another reason to include this simulator is that it may one day mature into a robust, practical, and competitive simulator if a community of open source developers and users grow around it. Berkeley Spice suffers in this regard as it is released under a restrictive license, and therefore, its continued development by the open source community never materialized.

Like the other circuit simulators, NGSpice also provides a number of `.OPTION` statements to control the numerical solving algorithms. Since NGSpice is based on Berkeley Spice, the options and models in NGSpice are identical to Berkeley Spice; however, NGSpice does not implement the `ITL3` and `ITL5` options.

2.2 Newton-Raphson Method

The Newton-Raphson method is a fairly simple yet powerful method for finding the roots of a real-valued function. As long as the initial guess of the solution lies close to the actual root, and the root of interest has a multiplicity of one, then this algorithm will converge quadratically. If the root has a multiplicity greater than one, the algorithm will converge linearly, except for some abnormal cases.

After an initial guess is made the algorithm will calculate the tangent of the function at that point. By extrapolating the tangent and determining where it crosses the independent axis the next guess of the solution can be found. This process is then iterated until certain convergence conditions are met, namely that the percentage change in the solution between two iterations is less than some predetermined value.

2.3 General Convergence Techniques

When dealing with problem circuits there are a number of tricks and techniques that can be employed to coax the numerical solvers into convergence. Some of the techniques lie in tweaking the operating parameters of the numerical solving algorithms, others involve slight modifications to the circuit to reduce the complexity of problem nodes, while even others employ alternate numerical methods outright. The following are some popular techniques.

2.3.1 Extra Iterations

All numerical algorithms include a limit on the number of iterations to perform; some circuits may simply not have a solution and so the algorithms will run infinitum. For some cases, the

convergence point may be just a few iterations away or the circuit may have the necessary conditions to cause slow convergence for the numerical algorithms. In these cases convergence will eventually occur given sufficient iterations.

2.3.2 Initial Guesses

One of the conditions for quadratic convergence in the Newton-Raphson algorithm is that an initial guess must lie close to the actual solution. While this may be trivial for simple one solution circuits, it is an important consideration when simulating circuits with multiple operating points. The Newton-Raphson algorithm will provide its own guesses but can only find one solution during each run. By providing guesses as to where other solutions may lie, the user can coax the simulators to converge to the other solutions of interest.

2.3.3 Homotopy Methods

An alternative is to use methods such as parameter variation, known as homotopy. By embedding a parameter, or varying an existing one such as the power supply voltage, the circuit can be reduced to a simpler solution that is easily solved. Then by iteratively varying this parameter and using the previous solution as an initial guess for the next, it is possible to eventually solve the original problem. The simulators evaluated in this paper all automatically invoke some form of homotopy methods when confronted with a difficult circuit to simulate. The methods used are GMIN stepping, source stepping, and a type of natural parameter homotopy.

GMIN stepping places shunt resistors from each node to ground. For a sufficiently large shunting conductance the circuit problem will degenerate to a simpler and solvable problem. By then iteratively reducing the shunting conductance and solving the circuit problem with the previous solution used as an initial conductance, a solution for the original circuit may be found. Source stepping is similar except all voltage and current sources are initially set to zero. They are then iteratively brought to full power with each solution used as an initial guess for the subsequent iteration, leading to a full circuit solution.

While these methods are quite powerful they will still fail in certain cases, such as at a branch, or bifubercation, in the path followed by the homotopy method. Bifubercation points arise as the circuit is able to produce multiple solutions. In these cases a more robust method is required to generate a solution, or the simulator must be tricked into solving for one solution only.

2.3.4 Circuit Modifications

Another class of options available to the designer when dealing with difficult circuits is to modify the circuit in a manner that will produce useful results comparable to the original problem. This may include such things as shunting problem nodes to ground through a sufficiently large resistance, turning various elements on/off, and building two-port equivalent models of selected sections. Often times the modified circuit may be useful in generating a solution that can be used as an initial condition in simulating the original problem circuit.

The problem may also lie in the device models chosen, including MOSFETs, BJTs, and ICs. Many ideal models may possess regions of discontinuity or "infinities" that are very unfriendly to the circuit simulator. Often the simulator will fail inexplicitly at various points due to these discontinuities in the models and can be avoided by either swapping for an alternate model or by adjusting the simulation sweep points to jump over trouble spots.

The designer must take care in evaluating the appropriate modifications and interpreting their results as they may be wildly different than expected. As is readily the case, a simulation tool is most useful when the solution is already known to the designer.

3 Characterization of Transistor Models

The transistor device is modeled by adjusting various real world parameters from their nonlinear equations. As such, the range of models vary from the very simple, often ideal but less accurate, to the very complicated, but more practical. To frustrate even further, the various Spice flavours may implement models differently. In this experiment, three standard models of the bipolar junction transistor (BJT) and the metal-oxide semiconductor field effect transistor (MOSFET) are used: the Ebers-Moll BJT, Shichman-Hodges MOSFET, and BSIM3 MOSFET. This section characterizes and compares their behaviour in Spice.

3.1 Ebers-Moll BJT Model

The Ebers-Moll model is the most basic fundamental and ideal BJT model and is appropriately numbered as Level 1 in the simulators. Figure 1 characterizes its behaviour.

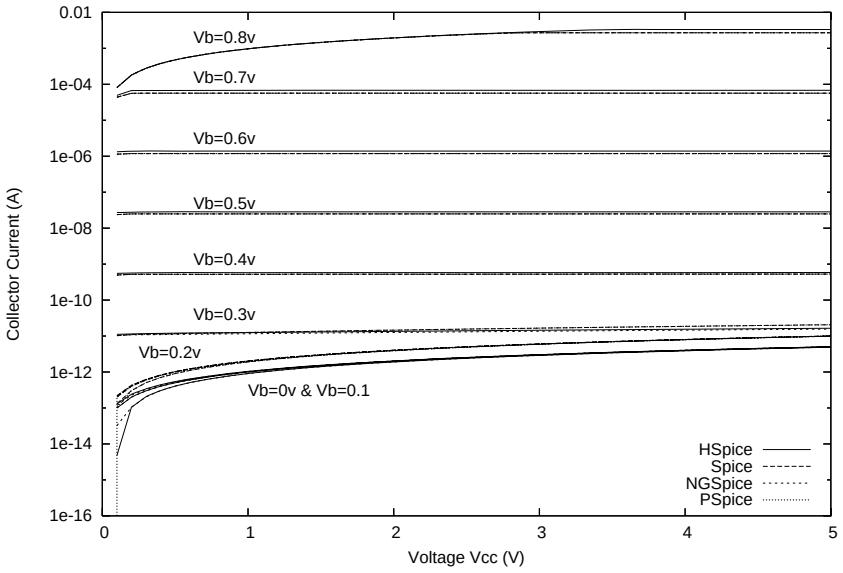


Figure 1: Ebers-Moll BJT Model Characterization

The characterization is fairly consistent across the four simulators. The notable difference is in the "elbow," at the transistor turn-on voltage, when the base voltage, V_b, is 0.2V or less.

3.2 Shichman-Hodges MOSFET Model

The Shichman-Hodges model is also the most basic of the MOSFET and is also numbered as Level 1. Its simulator characteristics are shown in Figure 2.

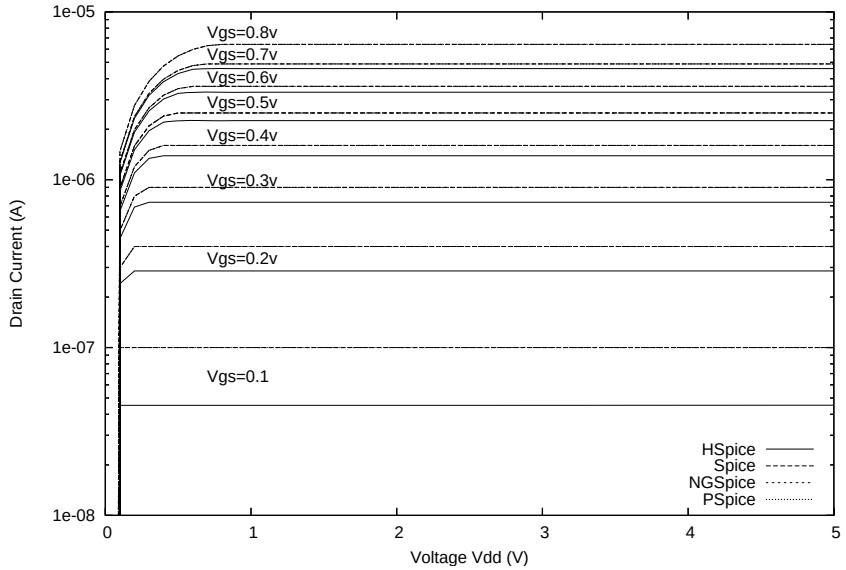


Figure 2: Shichman-Hodges MOSFET Model Characterization

Figure 3 shows the model characterization for the region where the gate-source voltage, $V_{gs} = 0$.

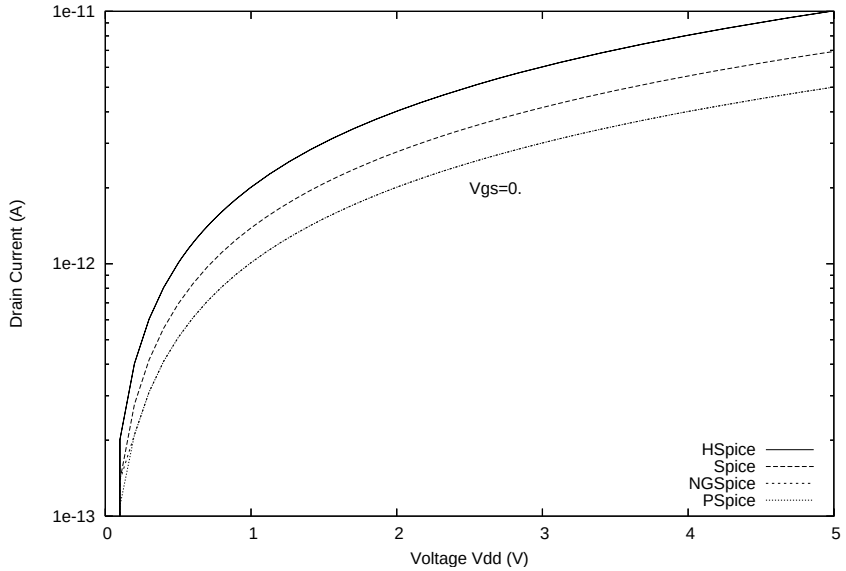


Figure 3: Shichman-Hodges MOSFET Model Characterization

For this model, the characterization shows that the implementations carried in the different Spice flavours can deviate quite a bit from each other.

3.3 BSIM3 MOSFET Model

The BSIM3 model was developed at Berkeley and has become an industry standard for modeling the MOSFET. Spice3f5 includes a fairly obsolete version of the BSIM3 model and so that flavour is not considered for this MOSFET model. HSpice provides compatibility with past versions of the BSIM3 and Figure 4 shows the characteristics of the two most recent, versions 3.3 (default) and 3.2.

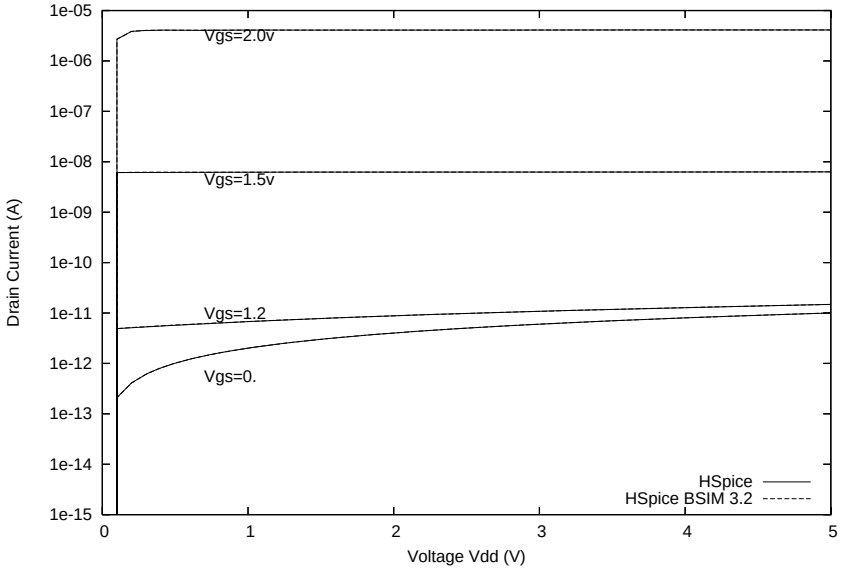


Figure 4: HSpice BSIM3 Default v3.3 and v3.2 MOSFET Model Characterization

The PSpice and NGSpice model characteristics are shown in Figure 5.

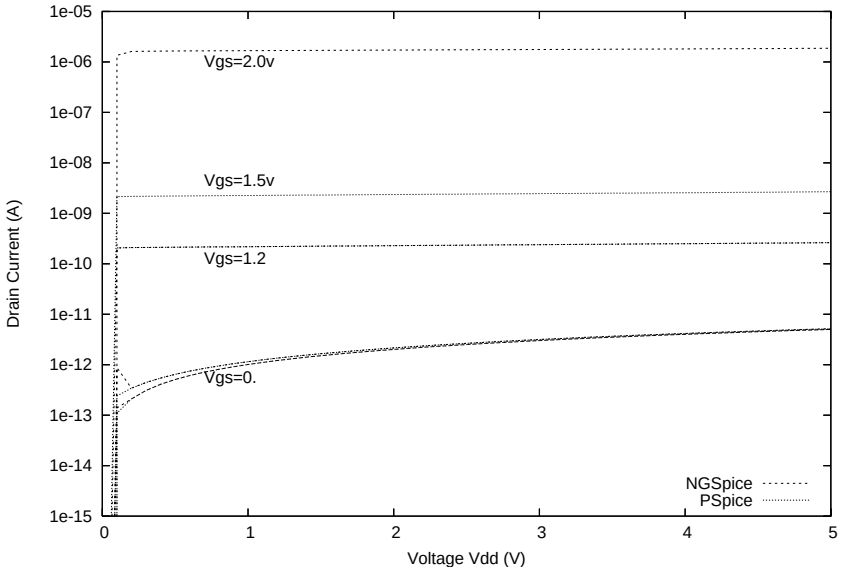


Figure 5: NGSpice and PSpice BSIM3 MOSFT Model Characterization

For the BSIM3 model, the simulator implementations characterized here are within close proximity of each other.

4 Circuits

Four different circuits using the described transistor models were chosen to test the strength of the numerical solvers in each of the simulators. The circuits are the input stage to the 741 opamp, a feedback circuit with good common mode rejection, a hybrid voltage reference, and the circuit with nine distinct operating points as popularized by Chua. For detailed comparison, full listings of the simulation outputs for all circuit nodes are available in Appendix B.

4.1 741 Opamp Input Stage

The input stage of the ubiquitous and elementary 741 operational amplifier [4] converts the differential input signal into single-ended form and shifts its DC level so the opamp output can swing positive and negative. Figure 6 shows the 741 input stage circuit.

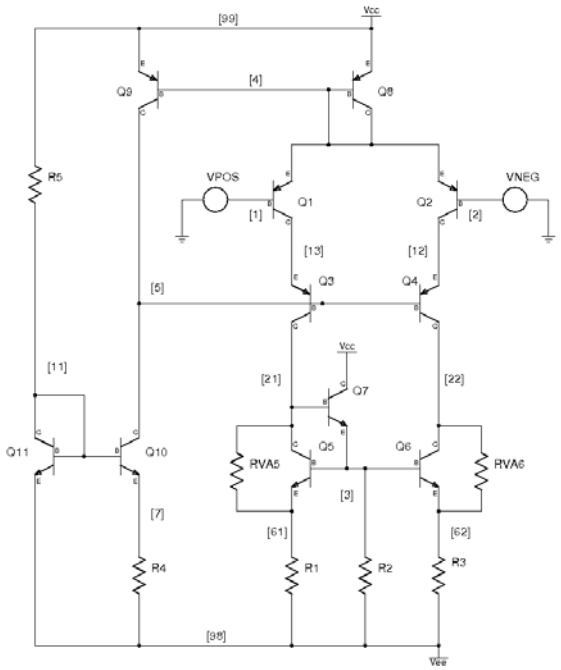


Figure 6: 741 Opamp Input Stage

The differential input is applied at the base terminals of transistors Q_1 and Q_2, which form a differential amplifier with Q_3 and Q_4. Transistors Q_5, Q_6, and Q_7 form the load circuit which acts as a current mirror. Biasing is conducted by the current mirror formed by Q_8 and Q_9, and by the Widlar current source formed by Q_{10} and Q_{11}. When the differential input terminals are balanced with equal voltages, the output is at 0V. With an even slightly unbalanced input, the output switches to the negative power rail.

The performance of the 741 opamp input stage is susceptible to the Early voltage effect on transistors Q_5 and Q_6, which we manually model by very large resistors RVA_5 and RVA_6, in parallel between the collectors and emitters of the two transistors, respectively. As suggested in [5], it is a worthwhile experiment to see how great the resistances could be increased to until the circuit behaviour is unexpected.

The circuit was simulated with the Ebers-Moll BJT model at various *RVA* resistances, with $RVA_5 = RVA_6$. A negligible input signal v_{iNEG} was applied at the negative terminal, with the positive held at zero. The output was initially conditioned to 6.0V. The operating points we obtained are summarized in Table 3.

Table 3: 741 Opamp Input Stage Operating Points

	Spice		HSpice		NGSpice	
RVA (Ω)	Output (V)	Iterations	Output (V)	Iterations	Output (V)	Iterations
1e12	-5.70	28	-5.81	51	-5.88	30
1e14	-6.34	28	-4.03	52	-6.46	29
1e16	-6.18	42	-4.01	52	-5.82	41
1e17	-5.99	83	-4.01	52	-6.18	87
1e18	-	-	-4.01	52	-6.81	979

At *RVA* = 1e18Ω and above, Spice fails to converge to a solution. While NGSpice does converge at this point, it requires nearly a thousand iterations to do so, and only after GMIN stepping has failed and source stepping has completed 32 iterations. HSpice does converge to an output above 1e18Ω even without use of GMIN stepping; however, given the exact match of the operating points found, and referring to the varying results from Spice and NGSpice, it is highly unlikely that these results can be confirmed. In general then, 1e17Ω is the largest *RVA* for nominal operation of the circuit, when the resistance models the Early effect.

4.2 Feedback Circuit with Good Common Mode Rejection

The opamp feedback circuit with good common mode rejection was originally presented by Banu *et al.* using MOSFETs [6], and later adapted into a BJT implementation by Melville *et al.* [5]. The circuit was also simplified to focus solely on the common mode feedback structure; the differential inputs were assumed to be null and the differential common mode feedback was collapsed into a single-ended feedback structure. Section 4.2.1 illustrates this circuit. For adequate comparison the original MOSFET version was simplified and reduced to the same architecture as the BJT implementation and is detailed in Section 4.2.2. As BJTs and MOSFETs exhibit similar behaviour we can expect similar behaviour between the BJT and MOSFET implementations of the common mode feedback circuit.

4.2.1 BJT Implementation

Figure 7 illustrates the BJT implementation of the common mode feedback circuit. Transistors Q_{1C}, Q_{1D}, Q_{2C}, Q_{3C}, Q_4, and Q_{4C} bias the output load transistor Q_3, the cascode transistor Q_8, and the differential pair Q_{5A} and Q_{5B}. The differential pair compares the output voltage against the desired common mode voltage V_{CM} and steer current provided by Q_{4C} in proportion to the

difference between the output voltage and V_{CM}. Transistors Q_2 and Q_{6B} mirror the current output from Q_{5B}, drawing current through the cascode transistor Q_8. This current sinks the current sourced by the differential transistor Q_{5A} and any excess current will flow into or out of the bias current through Q_1. A feedback path is thus created that will adjust the output voltage until the differential current flowing through Q_1 balances to zero, such that both Q_{5A} and Q_{5B} source equal currents, and with matched transistor properties, this will occur when the output voltage equals V_{CM}.

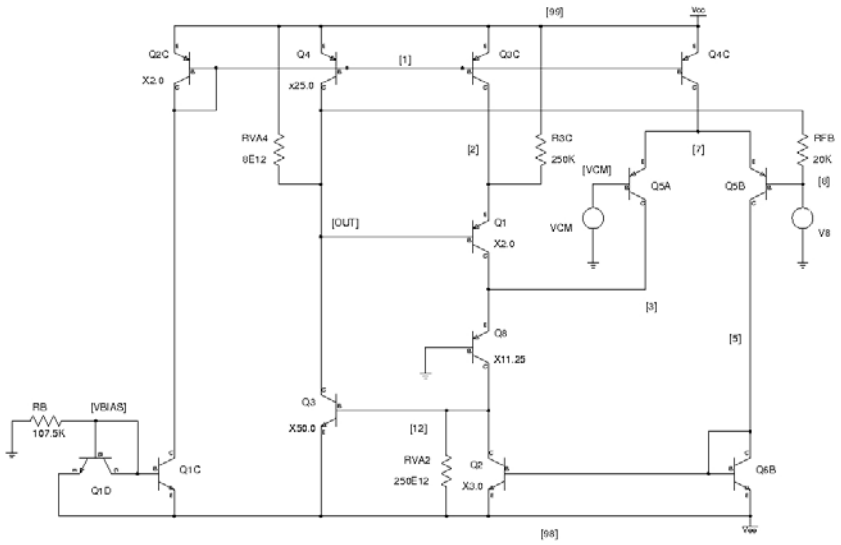
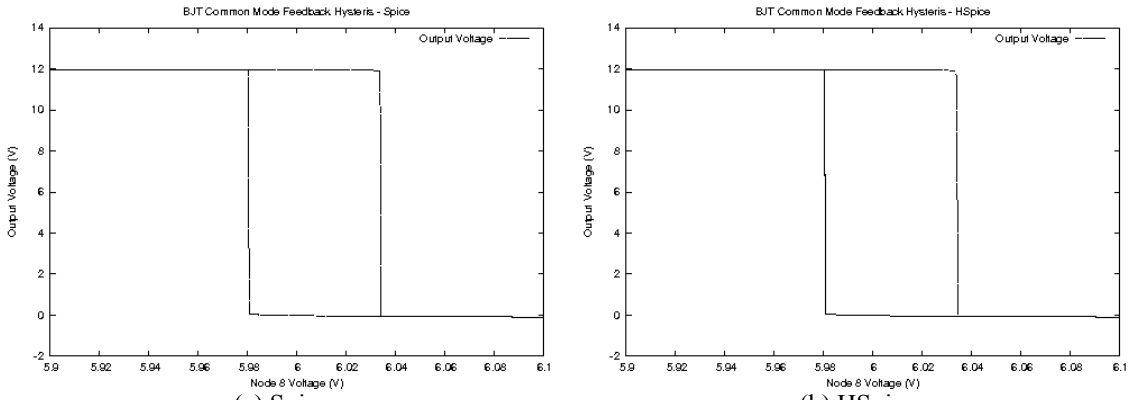
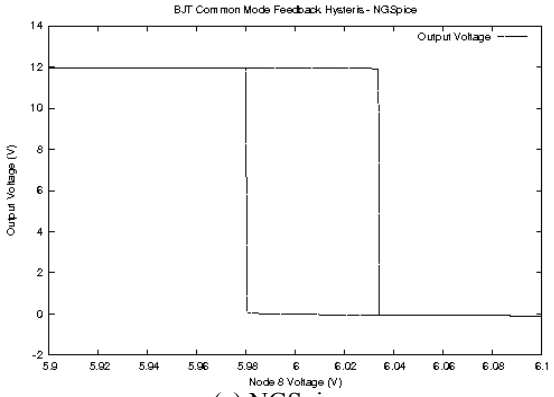


Figure 7: Common Mode Feedback Circuit BJT Implementation

The above analysis makes use of a simple linear approximation of the transistor's behaviour. Due to nonlinearities, the actual operation of the circuit does indeed exhibit some unexpected and interesting properties. By disconnecting the output voltage feedback to node 8 and instead sweeping this voltage around V_{CM}, a small hysteresis is found, as shown in Figure 8. An Ebers-Moll BJT model was used and V_{CM} was set to 6V. Interestingly all three simulators produced very similar results.



(a) Spice (b) HSpice



(c) NGSpice

Figure 8: BJT Common Mode Feedback Hysteresis

According to [5] at points inside the hysteresis, the circuit is capable of supporting three operating points: two of which are stable and are traced by the hysteresis curves while the third is unstable and lies somewhere in the middle of the hysteresis. To find the unstable point the circuit was biased to operate in the hysteresis region and provided with the appropriate initial condition. All three simulators converged to the same third operating point given in Table 4.

Table 4: Common Mode Feedback Circuit Operating Points

Operating Point (V)	OP1	OP2	OP3
Spice	11.95	-0.02	9.37
HSpice	11.94	-0.02	9.37
NGSpice	11.95	-0.02	9.37

4.2.2 MOSFET Implementation

The simplified version of Banu's *et al.* [6] common mode feedback circuit is shown in Figure 9. The simplification follows the same procedures and operates in the same manner as is outlined in the previous section.

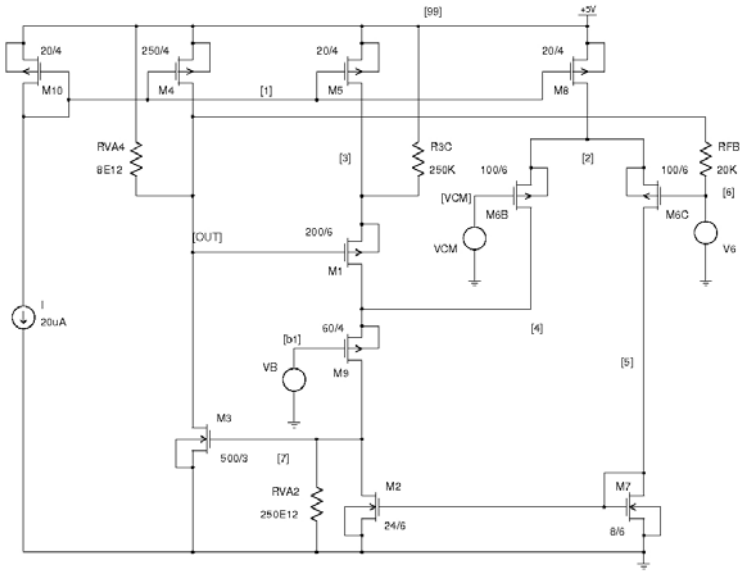
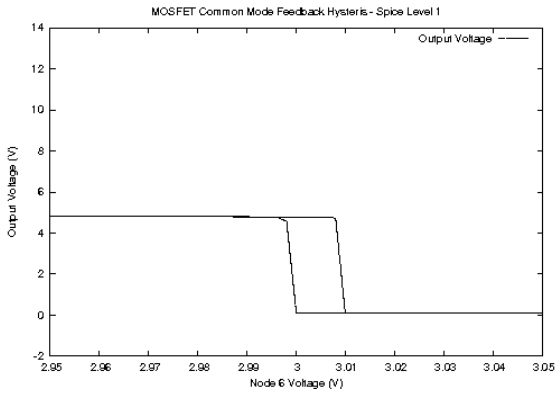
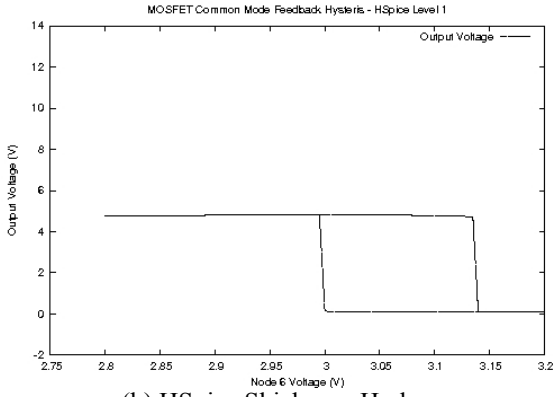


Figure 9: Common Mode Feedback Circuit MOSFET Implementation

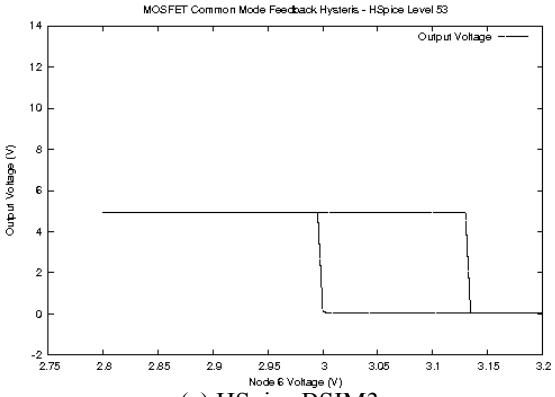
The MOSFET version was powered with a 5V supply and set to operate at a common mode voltage of 3V. Again, as with the BJT implementation, the input common mode voltage, V_6, was swept about 3V and a hysteresis was noticed as illustrated in Figure 10. Where available, higher order models were also used for comparison.



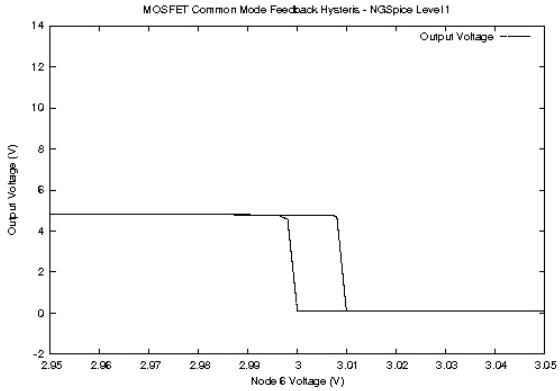
(a) Spice Shichman-Hodges



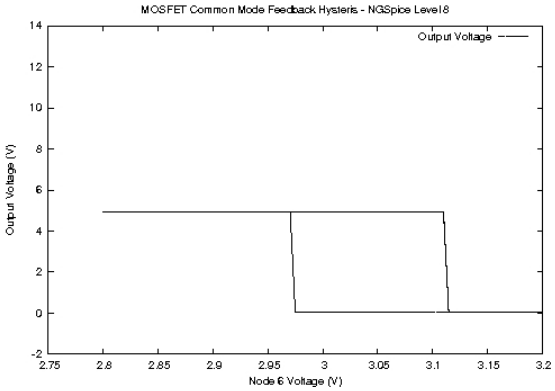
(b) HSpice Shichman-Hodges



(c) HSpice BSIM3



(d) NGSpice Shichman-Hodges



(e) NGSpice BSIM3

Figure 10: MOSFET Common Mode Feedback Hysteresis

Results for the MOSFET implementation varied considerably more than in the BJT case. As expected, the Spice and NGSpice Shichman-Hodges results were nearly identical, while results from the same model in HSpice were strikingly different. In the case of Spice and NGSpice, the hysteresis occurred in a much narrower region, between approximately 3.00V and 3.01V, while in HSpice this region stretched out considerably, from 3.0V to 3.15V.

Interestingly, though, the HSpice Shichman-Hodges results agree fairly well with the higher order HSpice and NGSpice BSIM3 model results. The hysteresis region for NGSpice's BSIM3

falls within approximately 2.97V to 3.12V, which compares with HSpice's Shichman-Hodges and BSIM3 hysteresis regions of roughly 3.0V to 3.15V.

Extrapolating from the BJT implementation, it is expected that a similar number of operating points should be found inside the hysteresis region for the MOSFET case. However, it proved difficult to find this third operating point in all simulators except for HSpice. As well, a close examination reveals some discrepancies between each simulator and model levels.

Nearly identical results were produced except in the number of iterations required to reach convergence, and strangely at node 1 for HSpice. Interestingly, the BSIM3 simulations produced very comparable results; however, considerable effort was required to converge with HSpice when simulating both the unstable and one of the stable operating points – more than 10,000 iterations were required to converge.

4.3 Hybrid Voltage Reference

The hybrid voltage reference circuit was examined by Banwell [7] and is shown in Figure 11. As a line regulator, its performance is best when the current through transistors Q_3 and Q_6 are equal. If transistors Q_6 and Q_8 and resistors R_5 and R_6 are matched, the line regulation is 0.7mV/V. As suggested by [5], a slight mismatch in R_5 and R_6 can improve the performance, but it could also lead to multiple operating points, which Banwell calls the circuit's "primary liability." A startup diode Q_{10} is then introduced to drive the circuit towards the desired stable DC operating point.

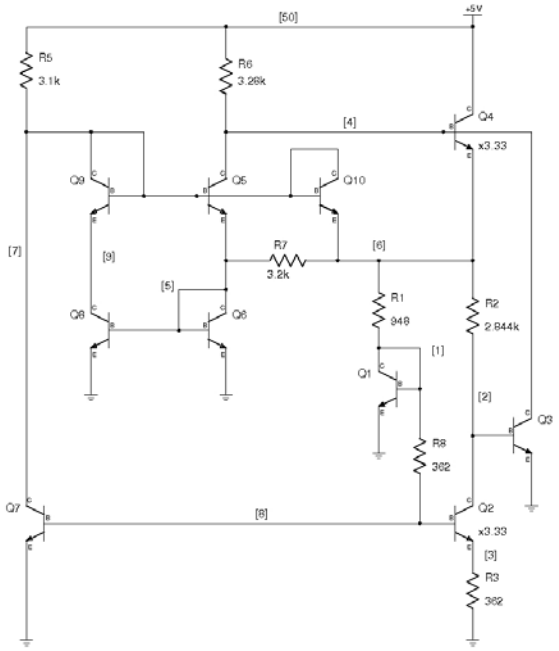


Figure 11: Hybrid Voltage Reference Circuit

To determine the operating points, this experiment mismatched R_5 and R_6, which were set to 3.1kΩ and 3.28kΩ, respectively. The startup diode Q_{10} was not included and three operating points were found, as summarized in Table 5.

Table 5: Hybrid Voltage Reference Operating Points without Startup Diode

Operating Point (V)	OP1		OP2		OP3	
	Output	Iterations	Output	Iterations	Output	Iterations
Spice	0.67	23	0.71	23	1.20	24
HSpice	0.66	27	0.71	22	1.19	10
PSpice	0.67	35	0.71	17	1.20	26
NGSpice	0.67	30	0.71	20	1.20	9

As a test of the effectiveness of the startup diode, the circuit was simulated again but with the diode included. Only one operating point was found by each of the four simulators in this case, that of "OP3." However, as shown in Table 6, the number of iterations to reach the stable operating point differs from the runs without the diode.

Table 6: Hybrid Voltage Reference Operating Point with Startup Diode

	Operating Point (V)	Iterations
Spice	1.20	20
HSpice	1.19	17
PSpice	1.20	15
NGSpice	1.20	13

While the iterations required to converge vary according to simulator, their resultant operating points are agreeable.

4.4 Chua's Circuit with Nine Distinct Operating Points

In a paper by Chua and Ushida [8], a circuit with nine distinct operating points was developed as a measure of the ability for circuit simulators and algorithms to solve difficult circuit problems. This circuit has since been used as a benchmark for various simulators and numerical techniques and as a result, its operating points are well known and understood. Figure 12 illustrates this circuit.

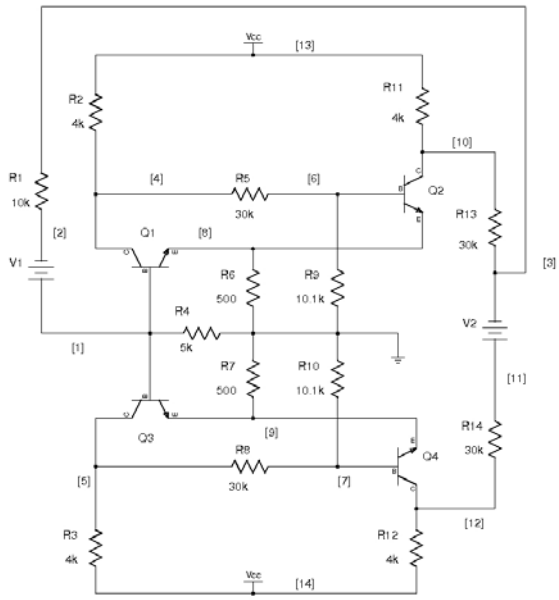


Figure 12: Chua's Circuit with Nine Distinct Operating Points

Results between all the simulators were again quite agreeable. No major discrepancies were found and in fact all the results were similar to within 1%. As well, there were no significant differences in the effort required by each simulator to reach convergence.

5 Discussion

Overall, the simulators performed well when faced with the difficult multiple operating point problem that the four test circuits present. The results gathered from Spice, HSpice, PSpice, and NGSpice agree to within some minute error, and in some cases, agree completely. However, HSpice provides a few curious examples which set it apart from the other flavours.

For the 741 opamp input stage, the operating points found from HSpice deviate quite a bit especially as the *RVA* resistance simulating the Early effect was increased. Also, HSpice exhibited a greater sensitivity to the switching effects even if the differential input was negligibly unbalanced. For the MOSFET implementation of the common mode feedback circuit, HSpice showed disagreement in the hysteresis region for an assumed equal model level, while the other flavours agreed within themselves. Also for this circuit, while the other flavours could not find the third unstable operating point, HSpice was able to do so.

From these results, it is clear that HSpice is set apart from its simulator brethren. We attribute this to its unique development as we described in Section 2. HSpice is generally regarded as an industry standad and thus, its numerical engine and features are well rounded and powerful. However, we cannot adequately claim that because of the attention given to HSpice, it is the better of the Spice flavours we have tested here. Instead, we have shed light on the argument that the simulators may provide conflicting results since their construction is also different.

Two circuits experienced notable convergence issues. NGSpice automatically invoked GMIN and source stepping for the 741 opamp input stage. For the more difficult operating points, GMIN stepping fails, and source stepping takes over. Interestingly, it should also be noted that for the 741 circuit, GMIN stepping in Spice does not yield the same solutions.

The BSIM3 implementation of the common mode feedback circuit in HSpice had convergence problems when solving for the unstable and surprisingly, one of the stable operating points. To compensate in these cases, the simulator itself enabled `DCON`, an "autoconvergence" feature that adjusted the `DV`, `GRAMP`, and `ITL1` options. On the autoconvergence try, solutions were found for both problem operating points, but only after 10,000 iterations.

As mentioned, Chua's nine operating point circuit is used as a benchmark to test simulators. All four of our Spice flavours performed well with this circuit and all nine operating points were found with relative ease. An interesting note here, however, is that when NGSpice invoked GMIN and source stepping after reaching its iteration limits, only one operating point was reached regardless of the starting conditions.

6 Conclusions

Our goal was to compare the performance of the numerical abilities of Spice3f5, HSpice, PSpice, and NGSpice by having them solve circuits known to possess multiple DC operating points. It was expected that the simulators would encounter convergence issues and techniques designed to overcome those problems were employed. While simpler techniques, such as the use of extra iterations and initial conditions, were used liberally by us, the simulators themselves invoked GMIN and source stepping on a couple of occasions.

The Spice-derived simulators have evolved considerably since the original Berkeley Spice was developed. More enhanced numerical solver engines and new features such as the convergence techniques, are built in so that even the more difficult circuits can be solved. In terms of performance, we have shown that the four simulators used in this investigation would be sufficient in solving circuits similar to those used here, provided that the user is willing to deal with convergence strategies. In terms of price, we have accessed both Spice3f5 and NGSpice free of charge. However, technical support is inconsistent when compared to the commercial versions of HSpice and PSpice.

While each simulator has its own advantages, it is hard for us to determine which is the best. In closing, we acknowledge that every situation will demand which simulator is required, and not discounting user preference, there are diverse simulators available to meet the needs of all.

7 References

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[3] R.A. DeCarlo and P.M. Lin, *Linear Circuit Analysis: Time Domain, Phasor and Laplace Transforms Approaches,* 2nd ed., New York: Oxford University Press, 2001.

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[5] R.C. Melville, Lj. Trajković, S.C. Fang, and L.T. Watson, "Artificial parameter homotopy methods for the DC operating point problem," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 12, no. 6, June 1993, pp. 861–877.

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[7] T.C. Banwell, "Performance limitations of low-voltage regulators using only n-p-n transistors," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 1, Jan. 1991, pp. 77–80.

[8] L.O. Chua and A. Ushida. "A switching-parameter algorithm for finding multiple solutions of nonlinear resistive circuits," *International Journal of Circuit Theory and Applications*, vol. 4, pp. 215-239, 1976.

Appendix A: Spice Descriptions of Circuits

```
opamp741.cir 741 opamp input stage circuit

****************
* signal sources
vpos   1       vcm    0  ac
vneg   2       vcm    -753.28u  dc
vcm    vcm     0      0

****************
* power supplies
vcc    99      0       dc      +12v
vee    98      0       dc      -12v

****************
* bjts
* qxxx nc      nb      ne   <ns>     mname
q1     4       1       13   13       ntype
q2     4       2       12   12       ntype
q3     21      5       13   13       ptype
q4     22      5       12   12       ptype
q5     21      3       61   61       ntype
q6     22      3       62   62       ntype
q7     99      21      3    3        ntype
q8     4       4       99   99       ptype
q9     5       4       99   99       ptype
q10    5       11      7    7        ntype
q11    11      11      98   98       ntype

****************
* resistors
* rxxx n1      n2      value
r1     61      98      1k
r2     3       98      50k
r3     62      98      1k
r4     7       98      5k
r5     99      11      39k
rva5   21      61      1e12
rva6   22      62      1e12

****************
* models
.model ntype npn
.model ptype pnp

****************
* analysis
.op
.options gmin=1e-22 abstol=1e-15 chgtol=1e-18 vntol=1e-9 itl1=50

.end
```

```
cmbias-bjt.cir difficult common mode bias circuit BJT

****************
* signal sources
vcomm  vcm     0       6.0 dc
v8     8       0       6.0 dc

****************
* power supplies
vcc    99      0       dc      +12v
vee    98      0       dc      -12v

****************
* bjts
* qxxx nc      nb      ne <ns> mname   area
q1     3       out     2   2   ptype   2
q1c    1       vbias   98  98  ntype   1
q1d    vbias   vbias   98  98  ntype   1
q2     12      5       98  98  ntype   3
q2c    1       1       99  99  ptype   2
q3     out     12      98  98  ntype   50
q3c    2       1       99  99  ptype   1
q4     out     1       99  99  ptype   25
q4c    7       1       99  99  ptype   1
q5a    3       vcm     7   7   ptype   1
q5b    5       8       7   7   ptype   1
q6b    5       5       98  98  ntype   1
q8     12      0       3   3   ptype   11.15

****************
* resistors
* rxxx n1      n2      value
rva2   12      98      250e12
rva4   99      out     8e12
r3c    99      2       250k
rb     vbias   0       107.5k
rfb    out     8       20k
*rva7  7       0       250e12

****************
* models
.model ntype npn  *level=8 *vers=503 avl=100
.model ptype pnp  *level=8 *vers=503 avl=100

****************
* analysis
.nodeset v(out)=1.19e+01
.op
.options post gmin=1e-24 *converge=3 *dchold=10 dcfor=10 *dcon=-1

.end
```

```
cmbias-mosfet.cir difficult common mode bias circuit MOSFET

****************
* signal sources
vcomm  cm      0     3.0
v6     6       0     3.0
vb1    b1      0     2.0

****************
* power supplies
vdd    99   0    dc    5
ibias  1    0    dc    20u

*****************
* mosfets
*mx   d  g  s  b  mname l       w
m1    4  ou 3  3  pt    l=6u    w=200u
m2    7  5  0  0  nt    l=6u    w=24u
m3    ou 7  0  0  nt    l=6u    w=500u
m4    ou 1  99 99 pt    l=4u    w=250u
m5    3  1  99 99 pt    l=4u    w=20u
m6b   4  cm 2  2  pt    l=6u    w=100u
m6c   5  6  2  2  pt    l=6u    w=100u
m7    5  5  0  0  nt    l=6u    w=8u
m8    2  1  99 99 pt    l=4u    w=20u
m9    7  b1 4  4  nt    l=4u    w=60u
m10   1  1  99 99 pt    l=4u    w=20u

****************
* resistors
* rxxx n1      n2      value
*rva2  7       0       250e12
*rva4  99      ou      8e12
*r3c   99      3       250e6
*rb    vbias   0       107.5k
rf     ou      6       20k

*****************
* models
.model nt nmos level=1
.model pt pmos level=1

****************
* analysis
.nodeset v(ou)=4.75
.op
.options gmin=1e-24 abstol=1e-24 chgtol=1e-18 reltol=0.000001 itl1=10000

.end
```

```
hybridref.cir hybrid voltage reference circuit

****************
* power supplies
vcc   50    0     dc    +5V

****************
* bjts
* qxxx      nc    nb    ne <ns>     mname
q1    1     1     0     ntype
q2    2     8     3     ntype
q3    4     2     0     ntype
q4    50    4     6     ntype
q5    4     7     5     ntype
q6    5     5     0     ntype
q7    7     8     0     ntype
q8    9     5     0     ntype
q9    7     7     9     ntype
q10   7     7     6     ntype

****************
* resistors
* rxxx      n1    n2    value
r1    6     1     948
r2    6     2     2.844k
r3    3     0     362
r5    50    7     3.1k
r6    50    4     3.28k
r7    5     6     3.2k
r8    1     8     362
*rload      6     0     1k

****************
* models
.model ntype npn

****************
* analysis
.nodeset v(6)=1.1
.op
.options post *converge=3

.end
```

```
nineop.cir Chua's circuit with nine operating points

****************
* power supplies
vcc1  13    0     12
vcc2  14    0     12
v1    1     2     10
v2    11    3     2

****************
* bjts
* qxxx      nc    nb    ne    <ns>  mname area
q1    4     1     8           ntype
q2    10    6     8           ntype
q3    5     1     9           ntype
q4    12    7     9           ntype

****************
* resistors
* rx  n1    n2    value
r1    3     2     10k
r2    13    4     4k
r3    5     14    4k
r4    1     0     5k
r5    4     6     30k
r6    8     0     0.5k
r7    9     0     0.5k
r8    5     7     30k
r9    6     0     10.1k
r10   7     0     10.1k
r11   13    10    4k
r12   14    12    4k
r13   10    3     30k
r14   11    12    30k

****************
* models
.model ntype npn is=1e-9 bf=100 br=1 temp=299

****************
* analysis

* OP1
*.nodeset v(1)=1.77 v(2)=-8.22 v(3)=-1.10 v(4)=1.46 v(5)=1.46 v(6)=0.36
   +v(7)=0.36 v(8)=1.38 v(9)=1.38 v(10)=10.45 v(11)=0.89 v(12)=10.69
* OP2
*.nodeset v(1)=1.78 v(2)=-8.21 v(3)=-2.55 v(4)=7.75 v(5)=1.47 v(6)=1.80
   +v(7)=0.37 v(8)=1.42 v(9)=1.39 v(10)=3.34 v(11)=-0.55 v(12)=10.52
* OP3
*.nodeset v(1)=1.76 v(2)=-8.23 v(3)=-2.93 v(4)=1.46 v(5)=9.85 v(6)=0.36
   +v(7)=1.82 v(8)=1.38 v(9)=1.44 v(10)=10.23 v(11)=-0.93 v(12)=1.57
* OP4
*.nodeset v(1)=1.81 v(2)=-8.18 v(3)=-4.41 v(4)=9.03 v(5)=7.95 v(6)=1.86
   +v(7)=1.84 v(8)=1.48 v(9)=1.46 v(10)=1.59 v(11)=-2.41 v(12)=2.89
* OP5
*.nodeset v(1)=1.84 v(2)=-8.15 v(3)=-4.30 v(4)=8.09 v(5)=8.09 v(6)=1.87
   +v(7)=1.87 v(8)=1.49 v(9)=1.49 v(10)=2.34 v(11)=-2.30 v(12)=2.57
```

```
* OP6
*.nodeset v(1)=1.78 v(2)=-8.21 v(3)=-2.55 v(4)=1.47 v(5)=7.75 v(6)=0.37
   +v(7)=1.80 v(8)=1.39 v(9)=1.42 v(10)=10.28 v(11)=-0.55 v(12)=3.57
* OP7
*.nodeset v(1)=1.76 v(2)=-8.23 v(3)=-2.93 v(4)=9.62 v(5)=1.46 v(6)=1.82
   +v(7)=0.36 v(8)=1.44 v(9)=1.38 v(10)=1.54 v(11)=-0.935 v(12)=10.47
* OP8
*.nodeset v(1)=1.81 v(2)=-8.18 v(3)=-4.44 v(4)=7.90 v(5)=9.34 v(6)=1.83
   +v(7)=1.85 v(8)=1.45 v(9)=1.47 v(10)=2.76 v(11)=-2.44 v(12)=1.58
* OP9
*.nodeset v(1)=1.72 v(2)=-8.27 v(3)=-4.76 v(4)=9.74 v(5)=9.96 v(6)=1.78
   +v(7)=1.78 v(8)=1.40 v(9)=1.40 v(10)=1.49 v(11)=-2.76 v(12)=1.50

.op
.options itl1=5

.end
```

Appendix B: Listings of Operating Point Results

B.1 741 Opamp Input Stage

RVA = 1e12

	SPICE	HSPICE	NGSPICE
V(1)	0.00	0.00	0.00
V(2)	0.00	0.00	0.00
V(3)	-11.34	-11.34	-11.34
V(4)	11.33	11.33	11.33
V(5)	-1.31	-1.30	-1.31
V(7)	-11.91	-11.91	-11.91
V(11)	-11.24	-11.24	-11.24
V(12)	-0.65	-0.65	-0.65
V(13)	-0.65	-0.65	-0.65
V(21)	-10.68	-10.68	-10.68
V(22) = OUT	-5.70	-5.81	-5.88
V(61)	-11.99	-11.99	-11.99
V(62)	-11.99	-11.99	-11.99
V(98)	-12.00	-12.00	-12.00
V(99)	12.00	12.00	12.00
Vcm	0.00	0.00	0.00
Iterations	28	51	30
GMIN	-	-	23
Source Step	-	-	-

RVA = 1e14

	SPICE	HSPICE	NGSPICE
V(1)	0.00	0.00	0.00
V(2)	0.00	0.00	0.00
V(3)	-11.34	-11.34	-11.34
V(4)	11.33	11.33	11.33
V(5)	-1.31	-1.30	-1.31
V(7)	-11.91	-11.91	-11.91
V(11)	-11.24	-11.24	-11.24
V(12)	-0.65	-0.65	-0.65
V(13)	-0.65	-0.65	-0.65
V(21)	-10.68	-10.68	-10.68
V(22) = OUT	-6.34	-4.03	-6.46
V(61)	-11.99	-11.99	-11.99
V(62)	-11.99	-11.99	-11.99
V(98)	-12.00	-12.00	-12.00
V(99)	12.00	12.00	12.00
Vcm	0.00	0.00	0.00
Iterations	28	52	29
GMIN	-	-	23
Source Step	-	-	-

RVA = 1e16

	SPICE	HSPICE	NGSPICE
V(1)	0.00	0.00	0.00
V(2)	0.00	0.00	0.00
V(3)	-11.34	-11.34	-11.34
V(4)	11.33	11.33	11.33
V(5)	-1.31	-1.30	-1.31
V(7)	-11.91	-11.91	-11.91
V(11)	-11.24	-11.24	-11.24
V(12)	-0.65	-0.65	-0.65
V(13)	-0.65	-0.65	-0.65
V(21)	-10.68	-10.68	-10.68
V(22) = OUT	-6.18	-4.01	-5.82
V(61)	-11.99	-11.99	-11.99
V(62)	-11.99	-11.99	-11.99
V(98)	-12.00	-12.00	-12.00
V(99)	12.00	12.00	12.00
Vcm	0.00	0.00	0.00
Iterations	42	52	41
GMIN	-	-	23
Source Step	-	-	-

RVA = 1e17

	SPICE	HSPICE	NGSPICE
V(1)	0.00	0.00	0.00
V(2)	0.00	0.00	0.00
V(3)	-11.34	-11.34	-11.34
V(4)	11.33	11.33	11.33
V(5)	-1.31	-1.30	-1.31
V(7)	-11.91	-11.91	-11.91
V(11)	-11.24	-11.24	-11.24
V(12)	-0.65	-0.65	-0.65
V(13)	-0.65	-0.65	-0.65
V(21)	-10.68	-10.68	-10.68
V(22) = OUT	-5.99	-4.01	-6.18
V(61)	-11.99	-11.99	-11.99
V(62)	-11.99	-11.99	-11.99
V(98)	-12.00	-12.00	-12.00
V(99)	12.00	12.00	12.00
Vcm	0.00	0.00	0.00
Iterations	83	52	87
GMIN	-	-	*fail*
Source Step	-	-	-

RVA = 1e18

	SPICE	HSPICE	NGSPICE
V(1)	-	0.00	0.00
V(2)	-	0.00	0.00
V(3)	-	-11.34	-11.34
V(4)	-	11.33	11.33
V(5)	-	-1.30	-1.31
V(7)	-	-11.91	-11.91
V(11)	-	-11.24	-11.24
V(12)	-	-0.65	-0.65
V(13)	-	-0.65	-0.65
V(21)	-	-10.68	-10.68
V(22) = OUT	-	-4.01	-6.81
V(61)	-	-11.99	-11.99
V(62)	-	-11.99	-11.99
V(98)	-	-12.00	-12.00
V(99)	-	12.00	12.00
Vcm	-	0.00	0.00
Iterations	-	52	979
GMIN	-	-	*fail*
Source Step	-	-	32

Notes:
1) NGSpice automatically invokes GMIN and source stepping.

B.2 Common Mode Feedback Circuit BJT Implementation

	OP1			OP2		
	SPICE	**HSPICE**	**NGSPICE**	**SPICE**	**HSPICE**	**NGSPICE**
V(1)	11.33	11.33	11.33	11.31	11.31	11.31
V(2)	11.98	11.98	11.98	0.68	0.68	0.68
V(3)	0.59	0.58	0.59	0.65	0.64	0.65
V(5)	-11.36	-11.36	-11.36	-11.33	-11.33	-11.33
V(7)	6.65	6.65	6.65	6.68	6.67	6.68
V(8)	6.00	6.00	6.00	6.00	6.00	6.00
V(12)	-11.96	-11.96	-11.96	-11.32	-11.32	-11.32
V(98)	-12.00	-12.00	-12.00	-12.00	-12.00	-12.00
V(99)	12.00	12.00	12.00	12.00	12.00	12.00
Vbias	-11.28	-11.28	-11.28	-11.28	-11.28	-11.28
Vcm	6.00	6.00	6.00	6.00	6.00	6.00
Vout	11.95	11.94	11.95	-0.02	-0.02	-0.02
Iterations	11	23	22	8	12	17

	OP3		
	SPICE	**HSPICE**	**NGSPICE**
V(1)	11.31	11.31	11.31
V(2)	10.05	10.04	10.05
V(3)	0.64	0.64	0.64
V(5)	-11.33	-11.33	-11.33
V(7)	6.68	6.67	6.68
V(8)	6.00	6.00	6.00
V(12)	-11.33	-11.33	-11.33
V(98)	-12.00	-12.00	-12.00
V(99)	12.00	12.00	12.00
Vbias	-11.28	-11.28	-11.28
Vcm	6.00	6.00	6.00
Vout	9.37	9.37	9.37
Iterations	6	44	12

B.3 Common Mode Feedback Circuit MOSFET Implementation

OP1	Basic -- Shichman-Hodges			BSIM3	
	SPICE	**HSPICE**	**NGSPICE**	**HSPICE**	**NGSPICE**
V(1)	4.37	3.90	4.37	2.68	2.75
V(2)	3.28	3.51	3.25	4.85	4.84
V(3)	3.16	3.22	3.06	4.76	4.79
V(4)	3.15	3.20	3.05	4.76	4.78
V(5)	0.87	0.98	0.87	2.12	2.06
V(6)	3.04	3.01	3.01	3.04	3.04
V(7)	2.58	2.63	2.49	4.20	4.22
V(99)	5.00	5.00	5.00	5.00	5.00
Vb1	2.00	2.00	2.00	2.00	2.00
Vcm	3.00	3.00	3.00	3.00	3.00
Vout	0.09	0.09	0.10	0.03	0.02
Iterations	7	19	23	10085	17

OP2	Basic -- Shichman-Hodges			BSIM3	
	SPICE	**HSPICE**	**NGSPICE**	**HSPICE**	**NGSPICE**
V(1)	4.37	3.90	4.37	2.68	2.75
V(2)	3.25	3.51	3.25	4.84	4.82
V(3)	4.89	4.99	4.89	5.00	5.00
V(4)	0.32	0.19	0.32	0.08	0.09
V(5)	0.86	0.98	0.86	2.10	2.01
V(6)	3.01	3.01	3.01	3.04	3.04
V(7)	0.29	0.17	0.29	0.06	0.07
V(99)	5.00	5.00	5.00	5.00	5.00
Vb1	2.00	2.00	2.00	2.00	2.00
Vcm	3.00	3.00	3.00	3.00	3.00
Vout	4.75	4.81	4.75	4.93	4.92
Iterations	9	14	30	25	27

OP3	Basic -- Shichman-Hodges			BSIM3	
	SPICE	**HSPICE**	**NGSPICE**	**HSPICE**	**NGSPICE**
V(1)	-	3.90	-	2.68	-
V(2)	-	3.51	-	4.84	-
V(3)	-	4.39	-	4.84	-
V(4)	-	0.69	-	2.52	-
V(5)	-	0.98	-	2.10	-
V(6)	-	3.01	-	3.04	-
V(7)	-	0.62	-	1.97	-
V(99)	-	5.00	-	5.00	-
Vb1	-	2.00	-	2.00	-
Vcm	-	3.00	-	3.00	-
Vout	-	3.90	-	3.02	-
Iterations	-	19	-	10094	-

Notes:
1) For HSpice trials over 10,000 iterations, autoconvergence was invoked.

B.4 Hybrid Voltage Reference without Startup Diode

OP1

	SPICE	HSPICE	PSPICE	NGSPICE
V(1)	0.66	0.65	0.66	0.66
V(2)	0.59	0.59	0.59	0.59
V(3)	0.01	0.01	0.01	0.01
V(4)	1.28	1.27	1.28	1.28
V(5)	0.78	0.77	0.78	0.78
V(6) = OUT	0.67	0.67	0.67	0.67
V(7)	1.55	1.54	1.55	1.55
V(8)	0.66	0.65	0.66	0.66
V(9)	0.78	0.77	0.78	0.78
V(50)	5.00	5.00	5.00	5.00
Iterations	23	27	35	30

OP2

	SPICE	HSPICE	PSPICE	NGSPICE
V(1)	0.68	0.68	0.68	0.68
V(2)	0.57	0.57	0.57	0.57
V(3)	0.02	0.02	0.02	0.02
V(4)	1.38	1.38	1.38	1.38
V(5)	0.78	0.77	0.78	0.78
V(6) = OUT	0.71	0.71	0.71	0.71
V(7)	1.55	1.54	1.55	1.55
V(8)	0.68	0.68	0.68	0.68
V(9)	0.78	0.77	0.78	0.78
V(50)	5.00	5.00	5.00	5.00
Iterations	23	22	17	20

OP3

	SPICE	HSPICE	PSPICE	NGSPICE
V(1)	0.75	0.75	0.75	0.75
V(2)	0.75	0.74	0.75	0.75
V(3)	0.06	0.06	0.06	0.06
V(4)	1.94	1.93	1.94	1.94
V(5)	0.76	0.76	0.76	0.76
V(6) = OUT	1.20	1.19	1.20	1.20
V(7)	1.52	1.51	1.52	1.52
V(8)	0.75	0.75	0.75	0.75
V(9)	0.76	0.75	0.76	0.76
V(50)	5.00	5.00	5.00	5.00
Iterations	24	10	26	9

B.5 Hybrid Voltage Reference with Startup Diode

	SPICE	HSPICE	PSPICE	NGSPICE
V(1)	0.75	0.75	0.75	0.75
V(2)	0.75	0.74	0.75	0.75
V(3)	0.06	0.06	0.06	0.06
V(4)	1.94	1.93	1.94	1.94
V(5)	0.76	0.76	0.76	0.76
V(6) = OUT	1.20	1.19	1.20	1.20
V(7)	1.52	1.51	1.52	1.52
V(8)	0.75	0.75	0.75	0.75
V(9)	0.76	0.75	0.76	0.76
V(50)	5.00	5.00	5.00	5.00
Iterations	20	17	15	13

B.6 Chua's Nine Operating Point Circuit

SPICE	OP1	OP2	OP3	OP4	OP5	OP6	OP7	OP8	OP9
V(1)	1.77	1.78	1.77	1.82	1.85	1.78	1.77	1.81	1.73
V(2)	-8.23	-8.22	-8.23	-8.18	-8.15	-8.22	-8.23	-8.19	-8.27
V(3)	-1.11	-2.56	-2.98	-4.41	-4.31	-2.56	-2.93	-4.44	-4.76
V(4)	1.46	7.75	1.46	9.05	8.09	1.47	9.63	7.91	9.76
V(5)	1.46	1.47	9.85	7.95	8.09	7.75	1.46	9.35	9.97
V(6)	0.37	1.80	0.37	1.86	1.87	0.37	1.82	1.83	1.78
V(7)	0.37	0.37	1.83	1.84	1.87	1.80	0.37	1.86	1.79
V(8)	1.39	1.43	1.38	1.48	1.50	1.40	1.44	1.46	1.40
V(9)	1.39	1.40	1.44	1.47	1.50	1.43	1.39	1.48	1.41
V(10)	10.46	3.34	10.24	1.59	2.34	10.29	1.54	2.77	1.50
V(11)	0.89	-0.56	-0.98	-2.41	-2.31	-0.56	-0.93	-2.44	-2.76
V(12)	10.69	10.52	1.54	2.90	2.58	3.58	10.48	1.58	1.50
V(13)	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
V(14)	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
Iterations	5	5	7	4	4	5	4	5	5

HSPICE	OP1	OP2	OP3	OP4	OP5	OP6	OP7	OP8	OP9
V(1)	1.77	1.78	1.77	1.82	1.85	1.78	1.77	1.81	1.73
V(2)	-8.23	-8.22	-8.23	-8.18	-8.15	-8.22	-8.23	-8.19	-8.27
V(3)	-1.11	-2.56	-2.98	-4.41	-4.31	-2.56	-2.94	-4.45	-4.76
V(4)	1.46	7.74	1.46	9.03	8.09	1.47	9.63	7.90	9.74
V(5)	1.46	1.47	9.85	7.95	8.09	7.74	1.46	9.34	9.95
V(6)	0.37	1.80	0.37	1.86	1.87	0.37	1.82	1.83	1.78
V(7)	0.37	0.37	1.82	1.84	1.87	1.80	0.37	1.86	1.79
V(8)	1.39	1.43	1.38	1.48	1.50	1.40	1.44	1.46	1.40
V(9)	1.39	1.40	1.44	1.47	1.50	1.43	1.39	1.48	1.41
V(10)	10.46	3.35	10.24	1.59	2.34	10.29	1.54	2.76	1.50
V(11)	0.89	-0.56	-0.98	-2.41	-2.31	-0.56	-0.94	-2.45	-2.76
V(12)	10.69	10.52	1.54	2.89	2.57	3.59	10.48	1.58	1.50
V(13)	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
V(14)	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
Iterations	6	6	8	5	6	6	5	6	6

PSPICE	OP1	OP2	OP3	OP4	OP5	OP6	OP7	OP8	OP9
V(1)	1.78	1.79	1.77	1.82	1.85	1.79	1.77	1.81	1.73
V(2)	-8.22	-8.21	-8.23	-8.18	-8.15	-8.21	-8.23	-8.19	-8.27
V(3)	-1.10	-2.56	-2.98	-4.41	-4.30	-2.56	-2.93	-4.44	-4.76
V(4)	1.46	7.77	1.46	9.06	8.10	1.47	9.63	7.91	9.78
V(5)	1.46	1.47	9.85	7.96	8.10	7.77	1.46	9.36	9.99
V(6)	0.37	1.81	0.37	1.86	1.87	0.37	1.83	1.84	1.78
V(7)	0.37	0.37	1.83	1.85	1.87	1.81	0.37	1.86	1.79
V(8)	1.39	1.43	1.38	1.48	1.49	1.40	1.44	1.46	1.40
V(9)	1.39	1.40	1.44	1.47	1.49	1.43	1.38	1.48	1.41
V(10)	10.46	3.33	10.24	1.59	2.35	10.29	1.54	2.78	1.49
V(11)	0.90	-0.56	-0.98	-2.41	-2.30	-0.56	-0.93	-2.44	-2.76
V(12)	10.69	10.52	1.54	2.91	2.59	3.57	10.48	1.58	1.50
V(13)	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
V(14)	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
Iterations	7	8	11	6	6	8	7	7	7

NGSPICE	OP1	OP2	OP3	OP4	OP5	OP6	OP7	OP8	OP9
V(1)	1.77	1.78	1.77	1.82	1.85	1.78	1.77	1.81	1.73
V(2)	-8.23	-8.22	-8.23	-8.18	-8.15	-8.22	-8.23	-8.19	-8.27
V(3)	-1.11	-2.56	-2.98	-4.41	-4.31	-2.56	-2.93	-4.44	-4.76
V(4)	1.46	7.75	1.46	9.05	8.09	1.47	9.63	7.91	9.76
V(5)	1.46	1.47	9.85	7.95	8.09	7.75	1.46	9.35	9.97
V(6)	0.37	1.80	0.37	1.86	1.87	0.37	1.82	1.83	1.78
V(7)	0.37	0.37	1.83	1.84	1.87	1.80	0.37	1.86	1.79
V(8)	1.39	1.43	1.38	1.48	1.50	1.40	1.44	1.46	1.40
V(9)	1.39	1.40	1.44	1.47	1.50	1.43	1.39	1.48	1.41
V(10)	10.46	3.34	10.24	1.59	2.34	10.29	1.54	2.77	1.50
V(11)	0.89	-0.56	-0.98	-2.41	-2.31	-0.56	-0.93	-2.44	-2.76
V(12)	10.69	10.52	1.54	2.90	2.58	3.58	10.48	1.58	1.50
V(13)	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
V(14)	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00	12.00
Iterations	8	8	10	7	6	8	7	8	8