Testing and Design-for-Testability Techniques for 3D Integrated Circuits

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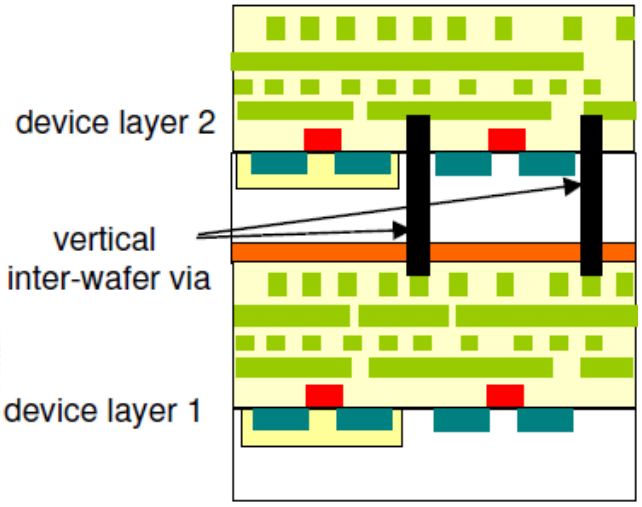

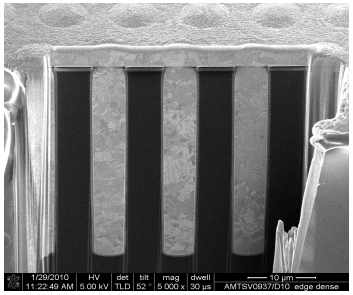

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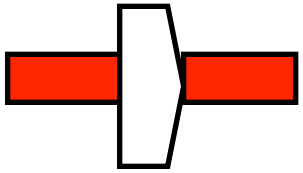
Acknowledgments

- Students: Brandon Noia, Sergej Deutsch, Mukesh Agrawal
- Collaborators: Erik Jan Marinissen (IMEC), Yuan Xie (Penn State Univ), Paul Franzon (NC State Univ), Sung Jyu Lim (Georgia Tech) Sreepad Pant (Georgia Tech)
- Sponsors: National Science Foundation, Semiconductor Research Corporation, Intel, Cisco

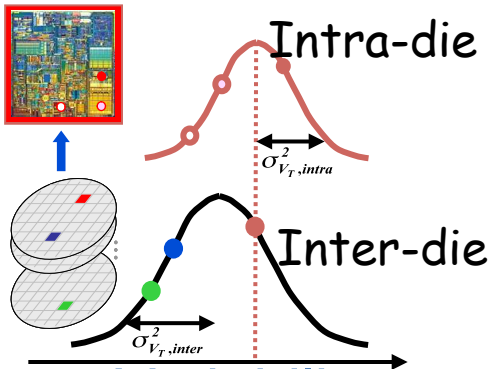
Outline

- Motivation
  - Drivers for 3D integration
- Technology Primer
  - Through Silicon Vias (TSVs), wafer thinning, stacking
- 3D IC Test Challenges
  - What to test? When to test? How to test?
  - Defects in 3D manufacturing
- Emerging Solutions
  - Pre-Bond Testing
  - Post-Bond Testing
- Conclusions

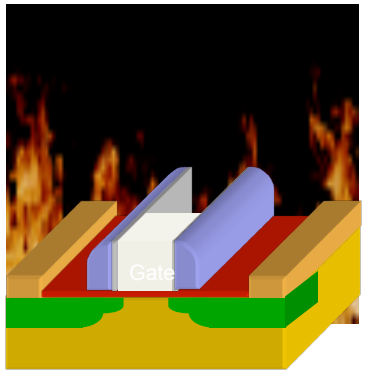
Roadblocks Ahead for IC Designers



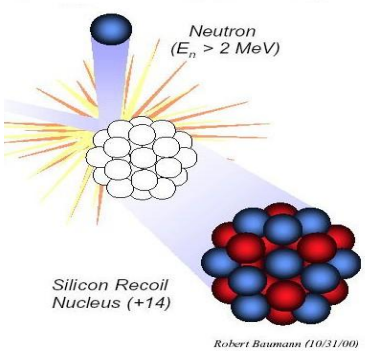
Wire Delay



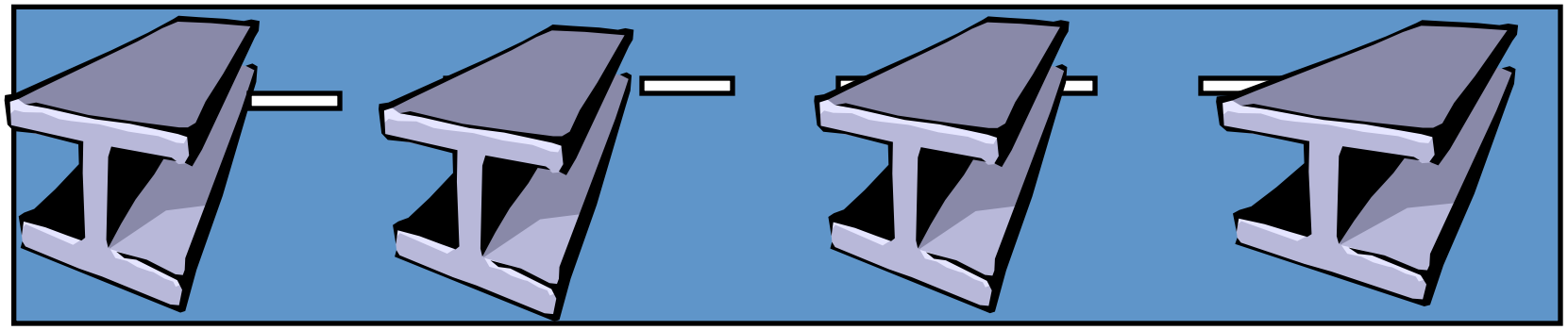
Variability



Power



Reliability

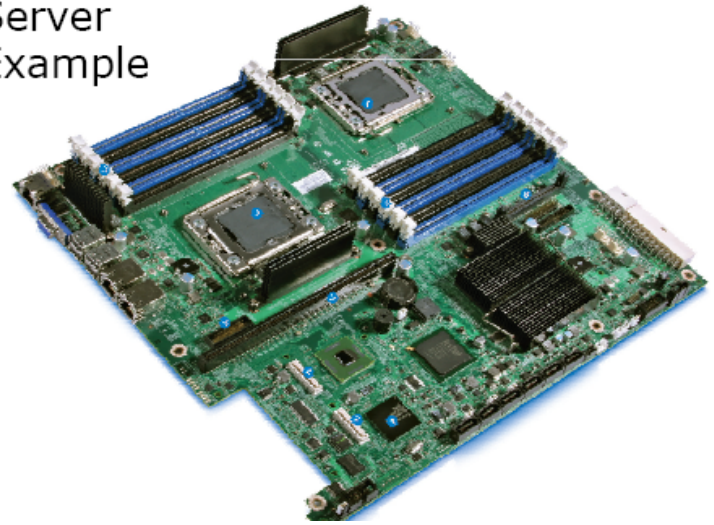


Motivation (Tanay Karnik, Intel)

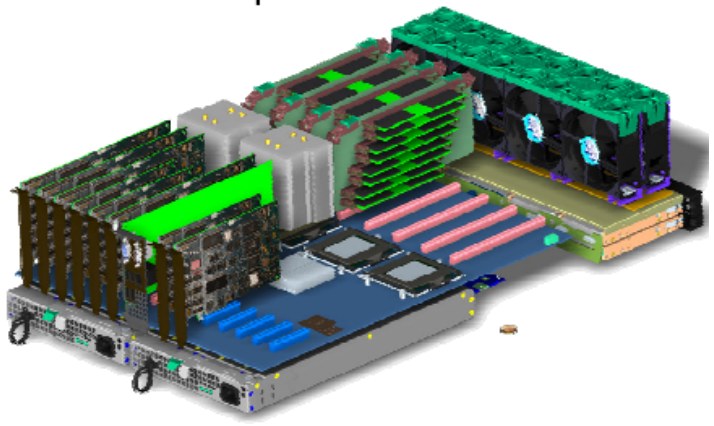
Microprocessor Bandwidth Needs

- As CPU core count increases, I/O bandwidth (BW) requirements will increase for all segments
- Current system bandwidth requirements (Y2010)
  - Client BW = ~50GB/s
  - Server BW = ~100GB/s
  - High-end Server BW = ~200GB/s

Server Example



High-End Server Example



High-end microprocessors will need 1 TB/s bandwidth by 2020

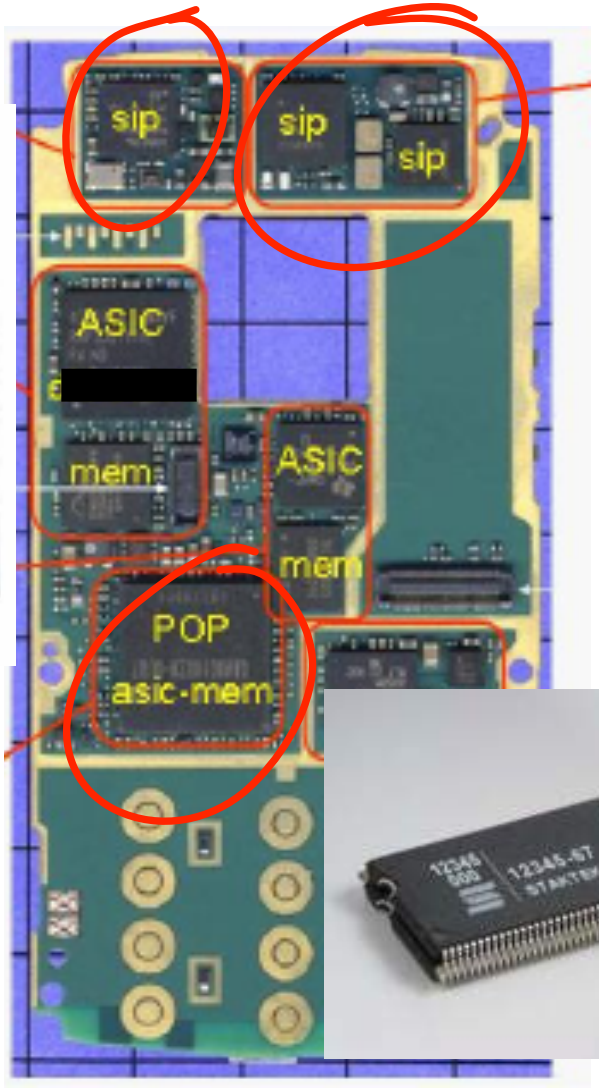
1TB/s x 20 pJ/bit = **160 W**

Vertical (3D) Integration isn't new!

We can also do heterogeneous stacks!

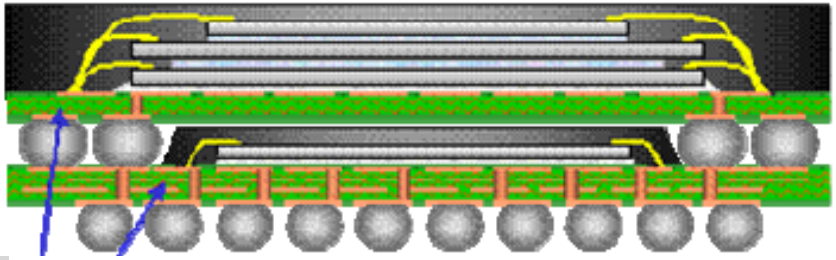
3D Stacking is not new

Nokia N95



Wire-bonding (WB) 3D stacking
(System-in-Package or SiP)

5MP Camera
GPS
Wireless
Bluetooth
Video player
Audio player
…

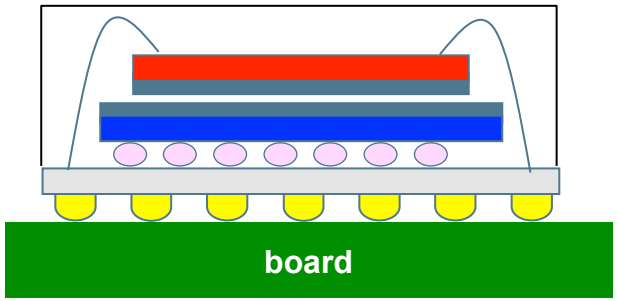


Package-on-Package (POP) 3D stacking

But Through-Silicon Vias (TSVs) are New!

Traditional stacking with:

• 3D chip stacking with wire-bonds:
Heterogeneous technologies
Dense integration, small footprint

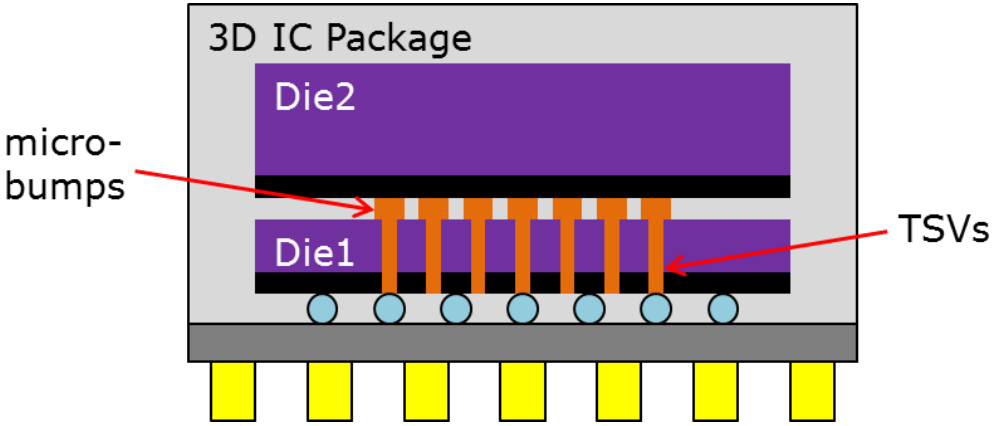


System-in-Package (SiP)

New stacking technology:

• Through-Silicon Vias (TSVs):
Metal vias that provide interconnects from front-side to back-side through silicon substrate

Diameter	5 µm
Height	50 µm
Aspect ratio	10:1
Minimum pitch	10 µm

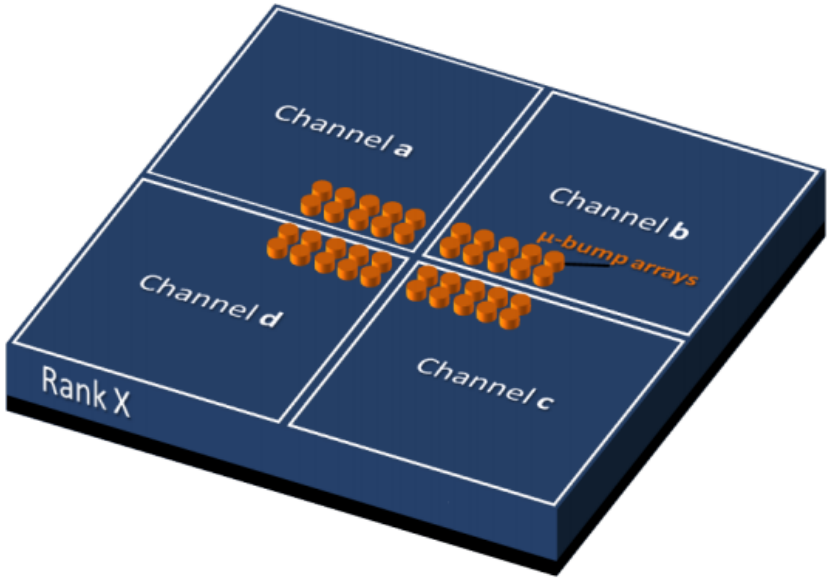


TSV-Based 3D-SIC

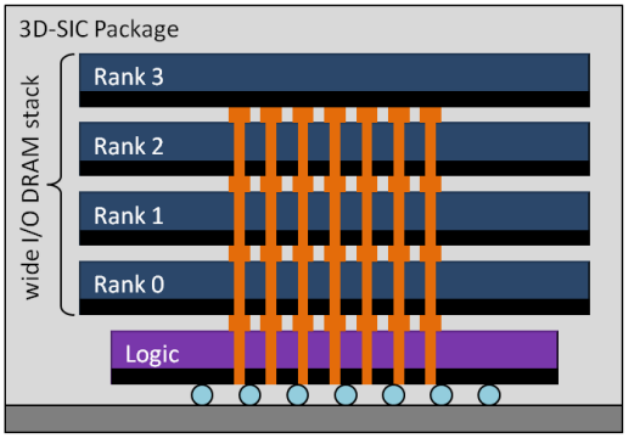
Applications

Memory-on-Logic (JEDEC Wide I/O DRAM)

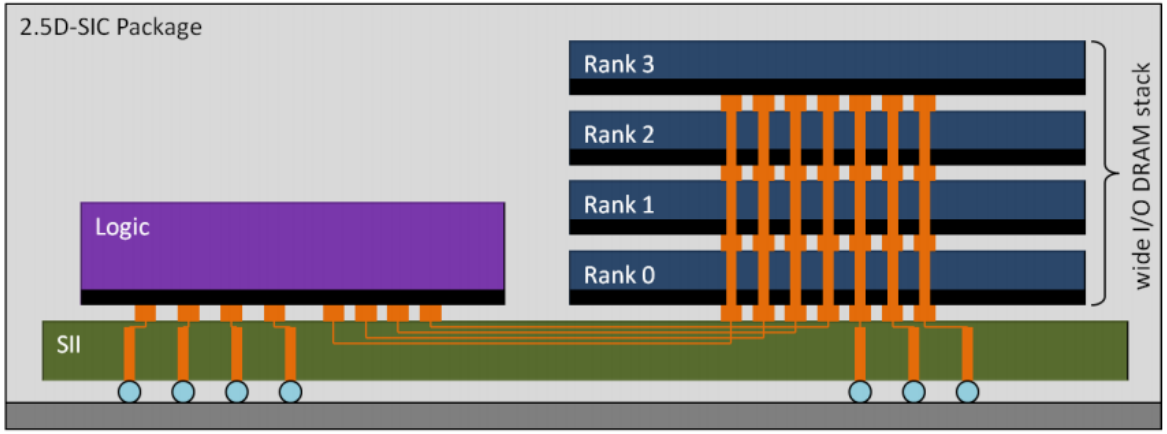
- 4 channels (*a*-*c*)
- 4 x 128 bit = 512 bit I/O
- 4 x 4.25 Gbytes/s = 17 Gbytes/s bandwidth
- Up to 4 stacked dies (Rank 0-3)



3D-SIC



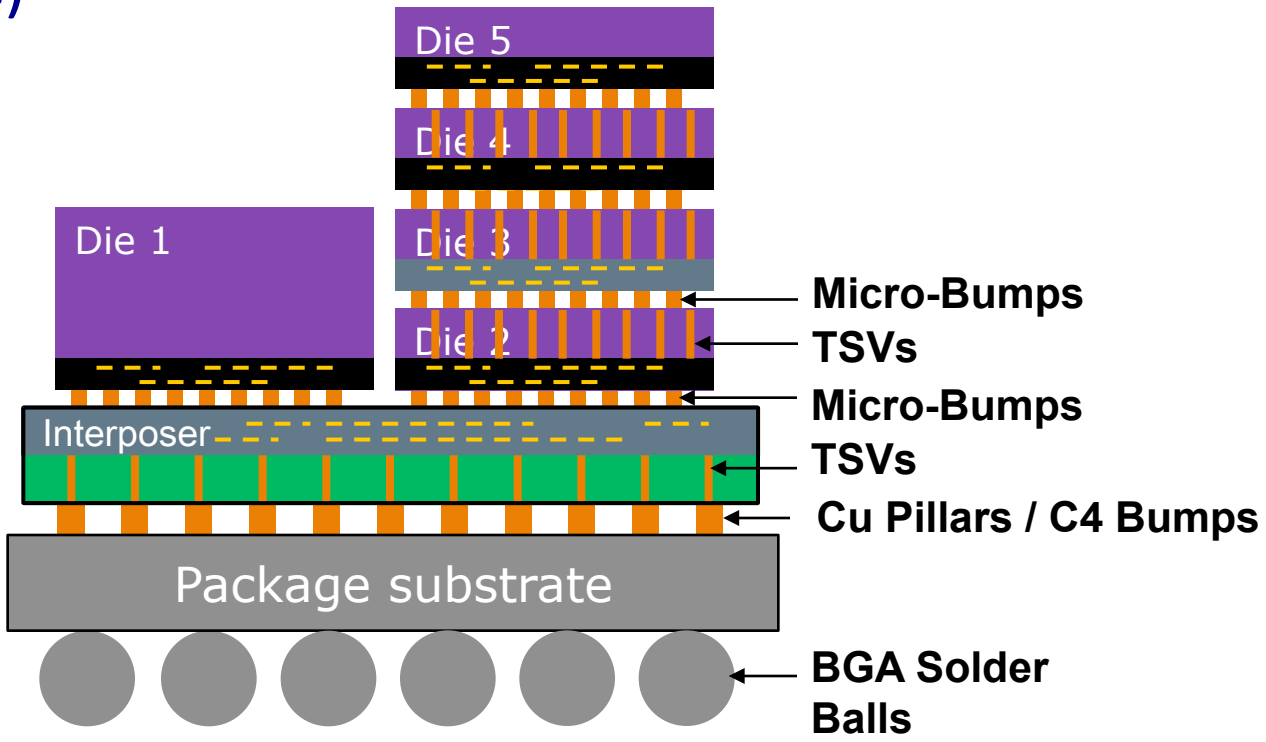
2.5D-SIC



Applications

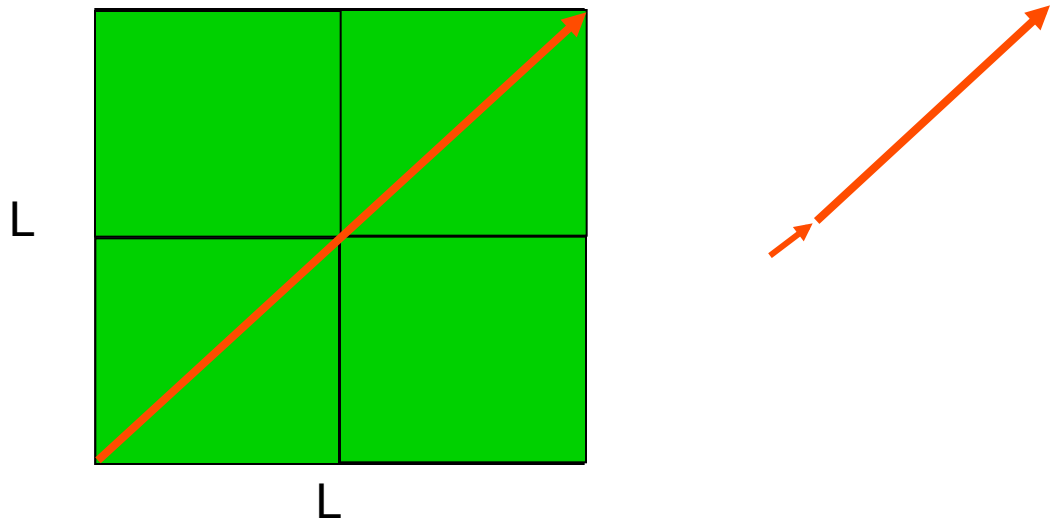
Future applications:

- Logic-on-logic
- Multi-tower stacks (both logic-on-logic and memory-on-logic)



Benefits of TSV based 3D ICs

- **Wire Length Reduction!**



- Performance/power improvement
- Higher throughput (bandwidth)
- Mixed-technology integration
- Potentially lower cost

TSV I/O (ESD) energy per operation: 7 pJ

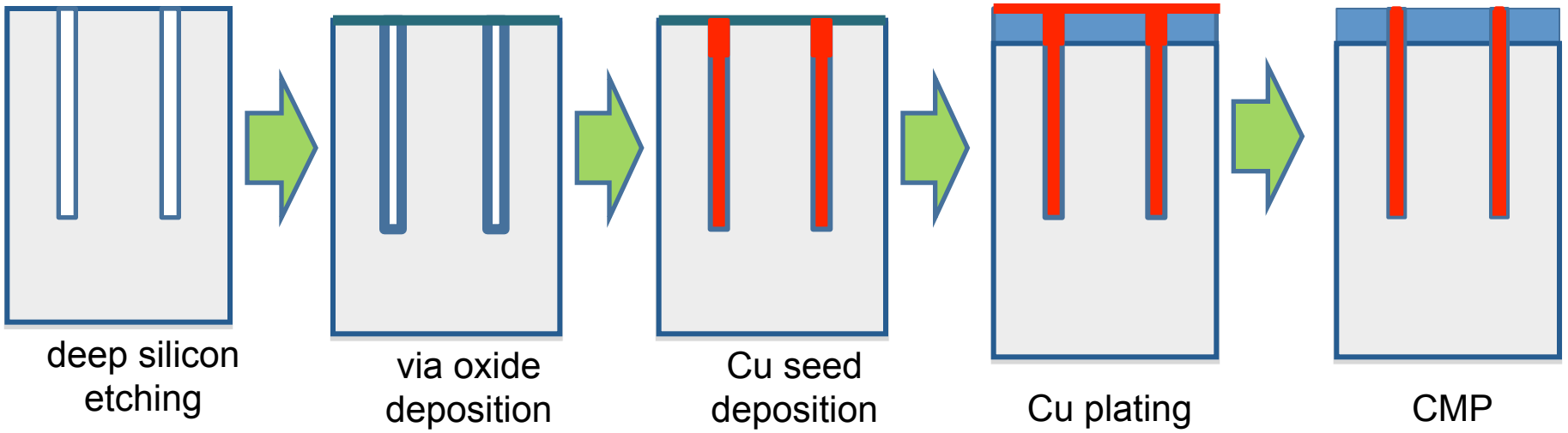
TSV I/O (no ESD) energy per operation: 2 pJ

What is TSV-Based 3D Integration?

And so these men of Hindustan
Disputed loud and long,
Each in his own opinion
Exceeding stiff and strong,
Though each was partly in the right
And all were in the wrong.

"The Blind Men and the Elephant" by John Godfrey Saxe (1816–1887).

TSV Formation, Wafer Thinning



Difficult to process wafers thinned below 100 microns

- Mount wafers on temporary wafer handlers (carriers)
- Thinning and backside processing

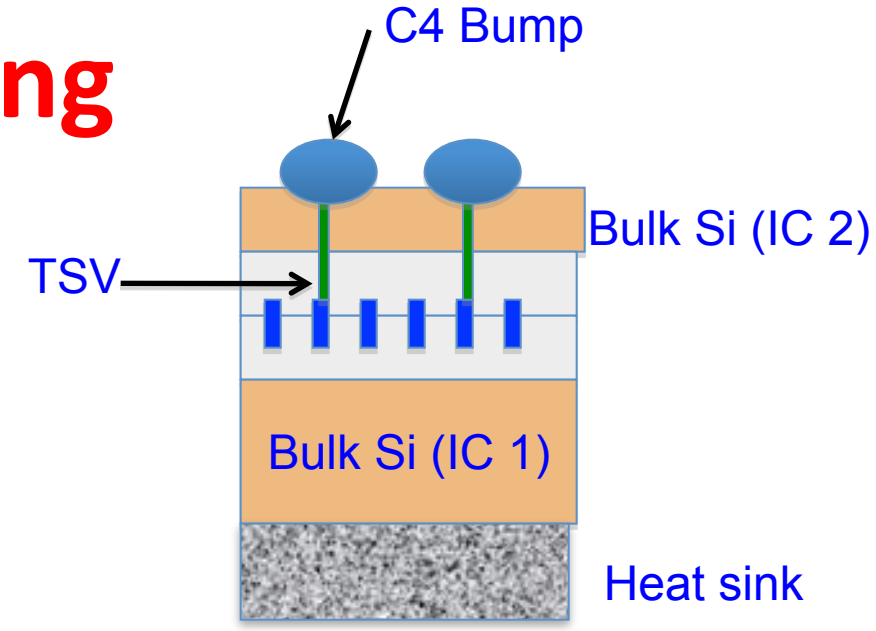
Option 1: Mount IC wafer face-down on carrier, bond “face-up” (B2F)

- Scalable solution, supports more stacked layers

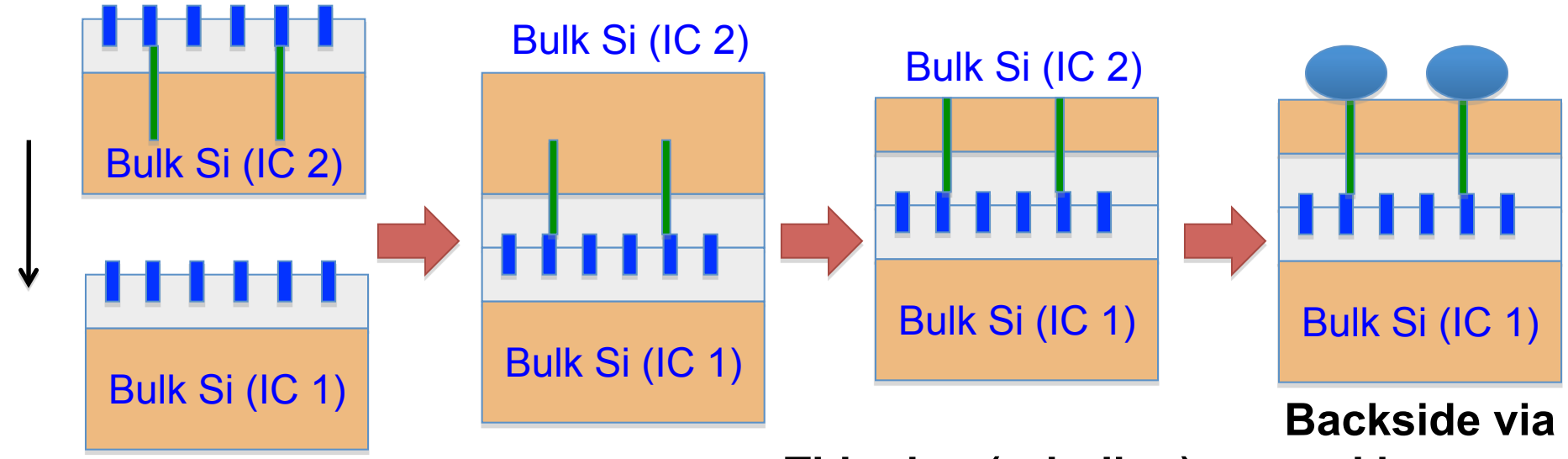
Option 2: Bond wafer to 3D stack in “face-down” configuration (F2F)

- More interconnects between active device on two layers
- Number of stacked dies limited to 2

Steps in F2F Bonding

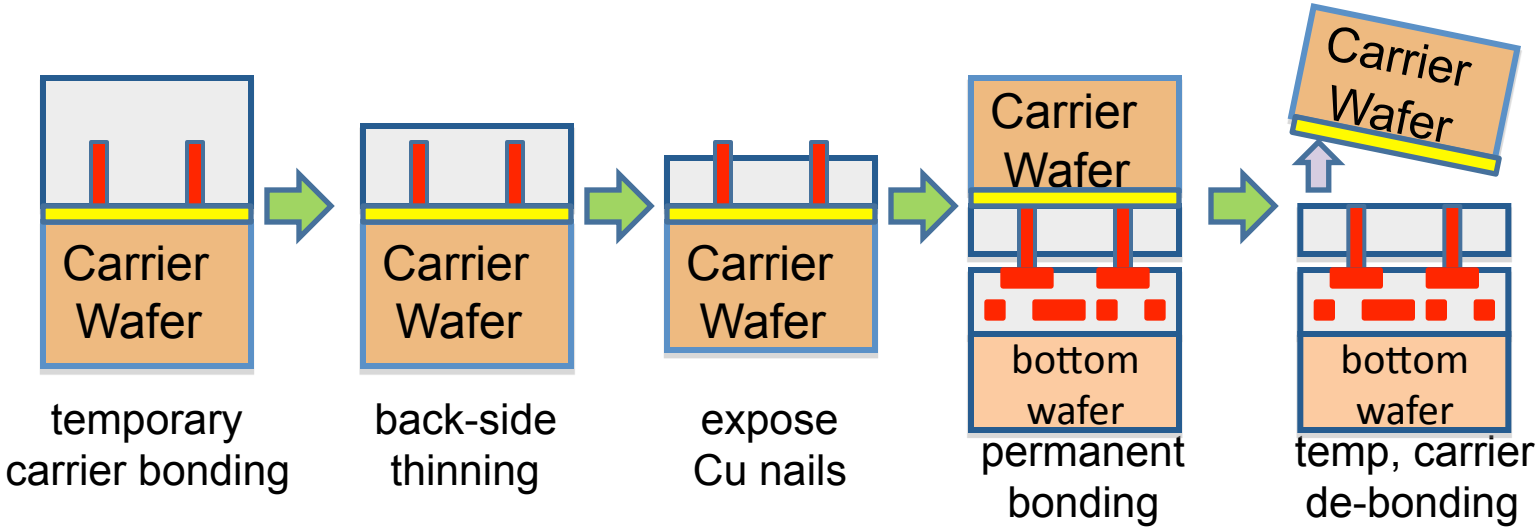


TSV prefabricated, but buried



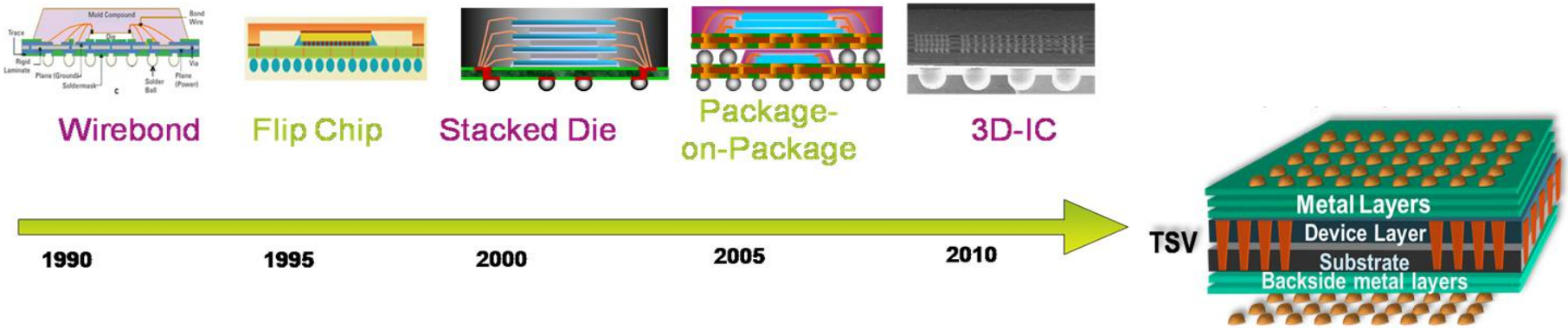
Align **Bonding** **Thinning (grinding)** **Backside via and bump process)**

Steps in B2F Bonding

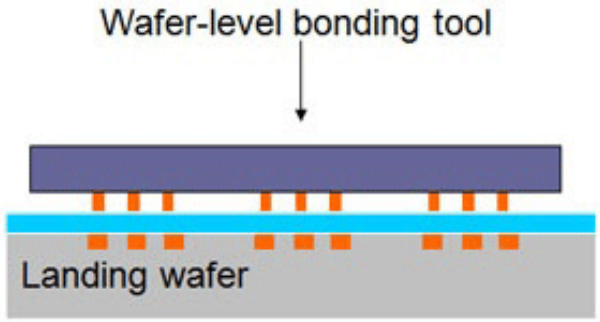


3D IC Integration and Options

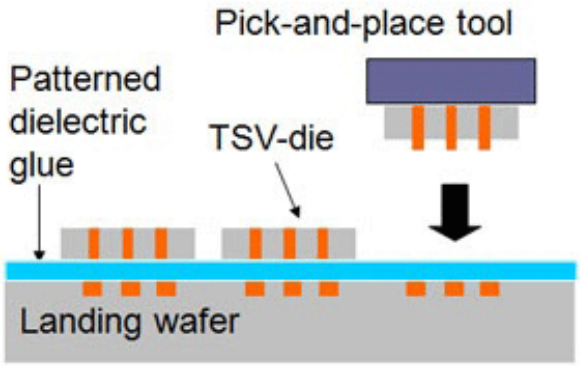
- Different vertical interconnects



- Different stacking strategies

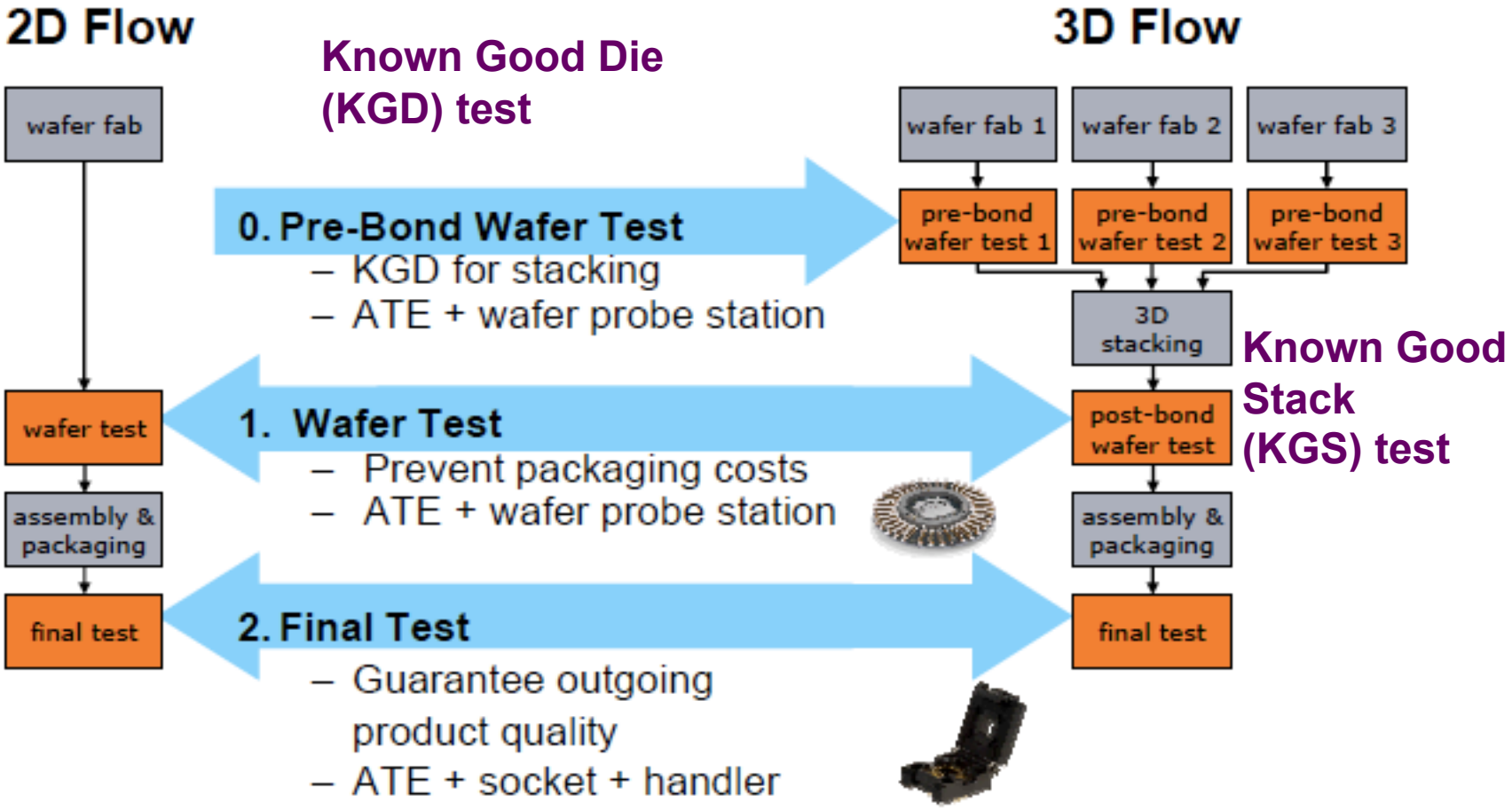


Wafer-to-Wafer



Die-to-Wafer

From Two to Three (or More?) Test Insertions



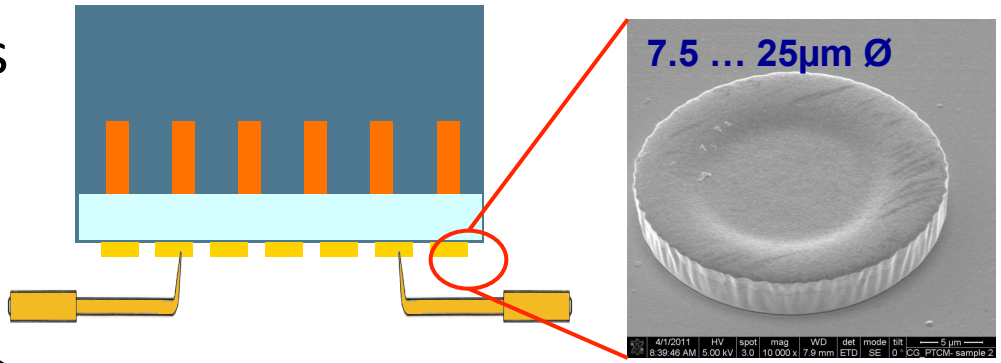
Test Content, Test Delivery, Test Resource Optimization and Reuse (Cost Minimization)

Key Questions

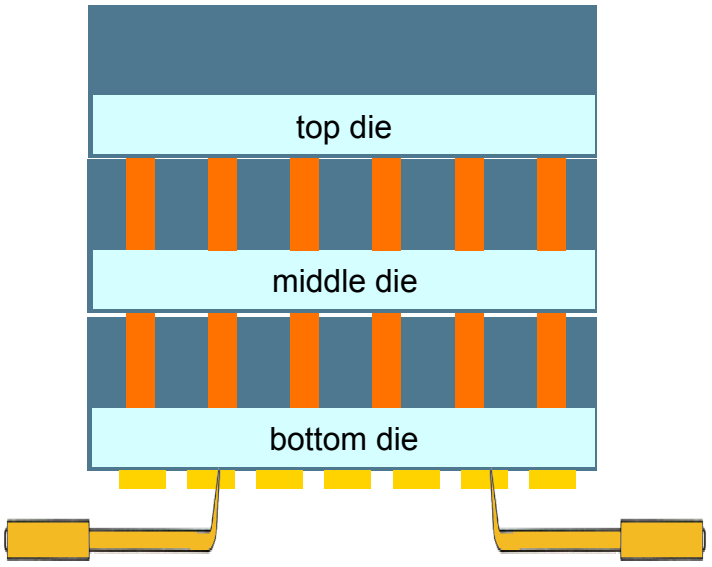
- What is different from today's ICs?
- What are the major roadblocks/show-stoppers?
- How much can we leverage from today's solutions and what needs to be developed from scratch?
- Determine appropriate test content (what to test?)
  - Pre-bond (known good die): Types of tests for TSVs and die logic
  - Post-bond: TSVs, die logic (cores and memories), tests for failing new defect types
- Determine test delivery pathways (how to test?)
- Select test flows: cost/benefit analysis (when to test?)

3D Test Challenges

- Micro-bump probe access: Current technology is not able to probe on micro-bumps/TSVs
  - Probe needles much larger than TSV/micro-bump size and pitch
- Probe card applies a force (weight) of 3-10 g per probe ⇒ probe force (weight) per wafer as high as 60-120 kg!
  - TSVs have low fracture strength
- Post-bond access: No direct access to non-bottom dies
- New defects due to TSV manufacturing process



[IMEC]

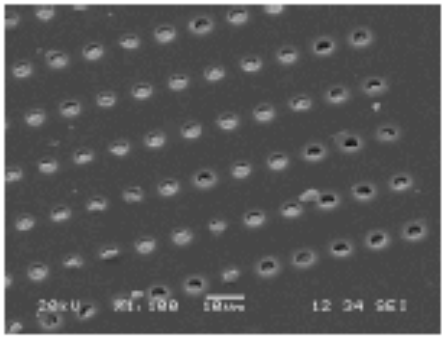


New Defect Types

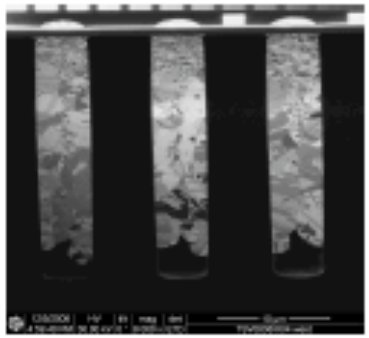
- Alignment, stacking, and thinning: c
- Foreign particles caught betwee
  - Voids, peeling, and delaminat
- Wafers must be precisely aligned for bo
  - Alignment problems lead to imperfect via connections
- Edge effects
  - Inter-wafer gap greater at the edges (weaker bond)
  - Bonded edges vulnerable to chipping, peeling, delamination
- Cracking during the stacking process: loading forces, backside grinding, die thinning
- Random open defects: dislocations, oxygen trapped on the surface, voids formation, and mechanical failures

Known good stack (KGS) test needed!

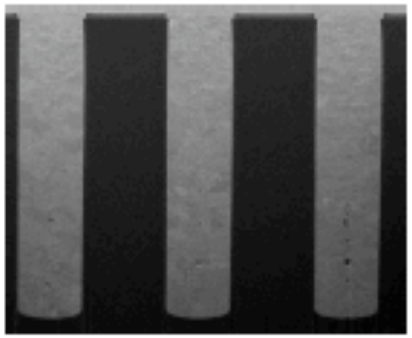
TSV Testing



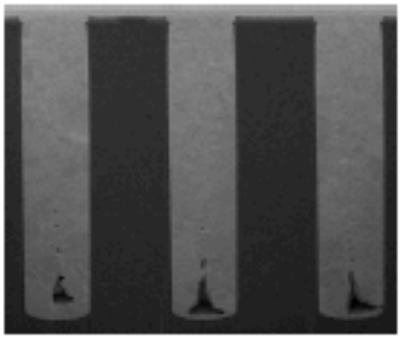
Improperly filled TSVs



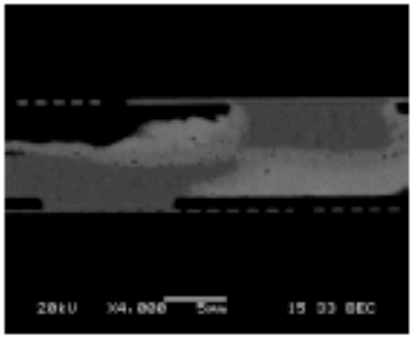
Insufficiently filled TSVs



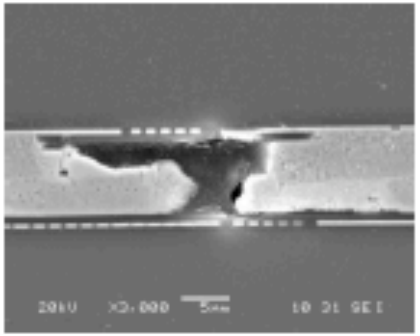
Micro-voids on TSV axis (quasi-conformal filling)



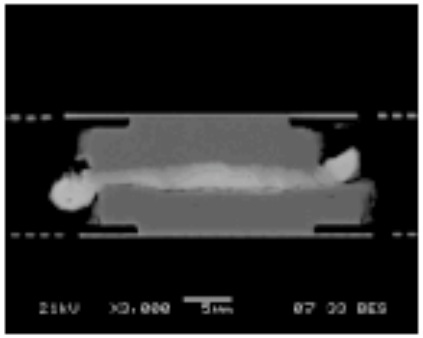
Micro-voids on TSV axis + large voids at bottom



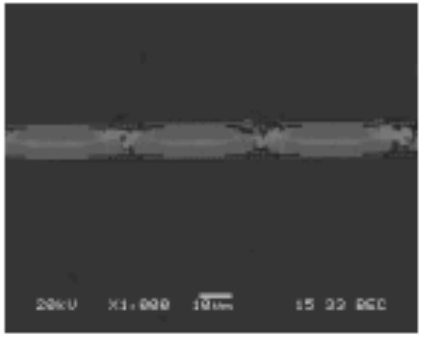
Misalignment



Misaligned bumps, almost-short with neighbors



Improperly soldered micro bumps



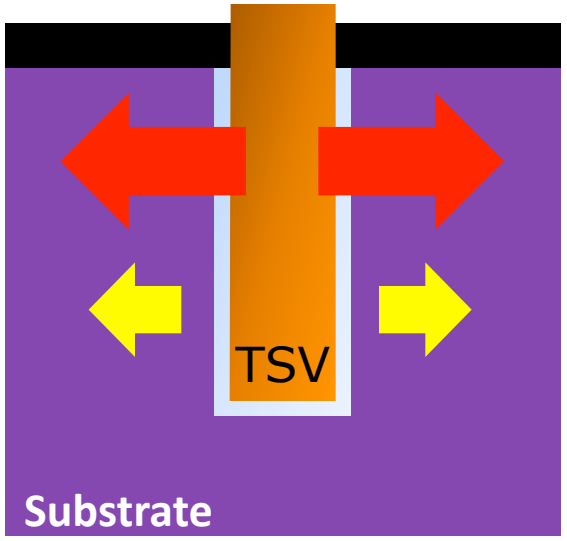
Shorts due to Sn squeezing

Examples of TSV Defects (IMEC, Belgium)

- How to test the TSVs? Pre-bond, post-bond
  - Underfill, pinhole defects, opens: pre-bond
  - Misalignment, mechanical/thermal stress: post-bond thermal effects
  - Boundary scan solution: flops at both ends? Functional tests?

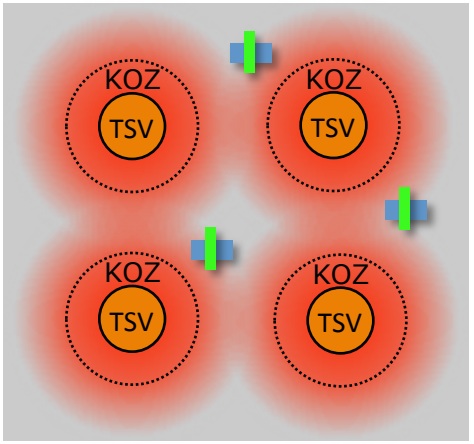
Thermo-Mechanical Stress due to TSVs

- Coefficient of Thermal Expansion mismatch:
  - $CTE_{Cu} = 17 \times 10^{-6}\ K^{-1}$
  - $CTE_{Si} = 3 \times 10^{-6}\ K^{-1}$
- Residual stress in Si



Consequences:

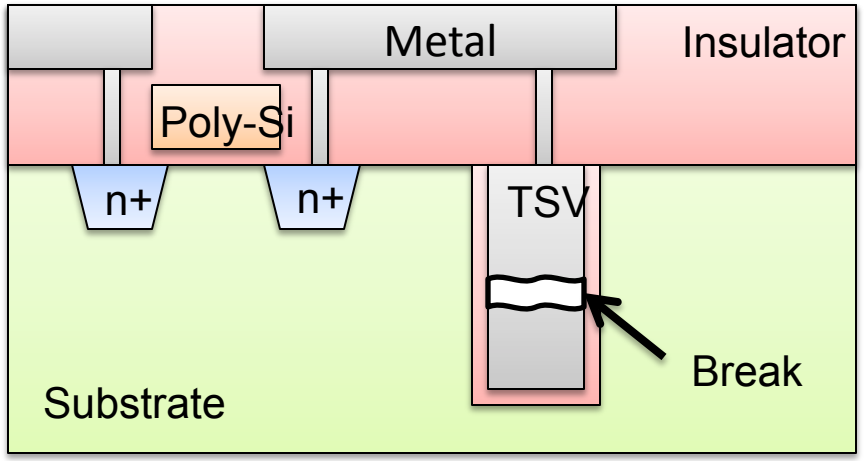
- Stress-induced defects
  - Cracks
  - Voids
- Mobility variation

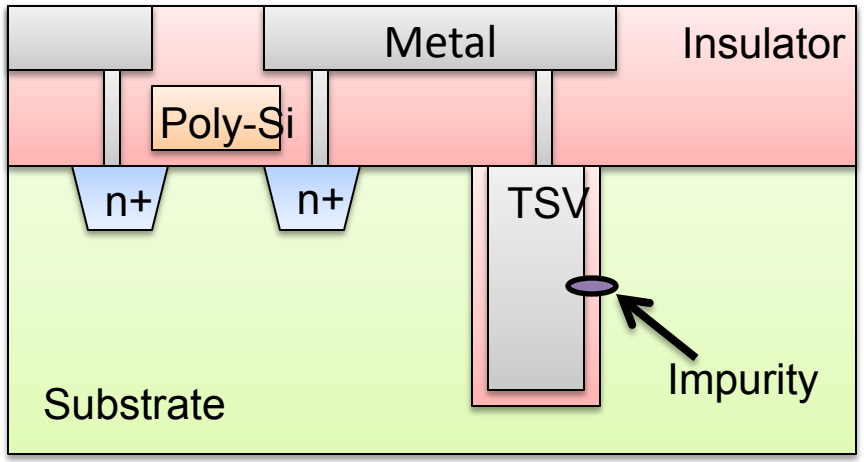


- Variations affect critical paths: Delay test patterns?
- TSV-induced stress failure in wires (electromigration)
- Microbump-induced stress: +40% current shift in nFET transistors, open defects

Pre-Bond Testing: TSV Defects and Capacitance

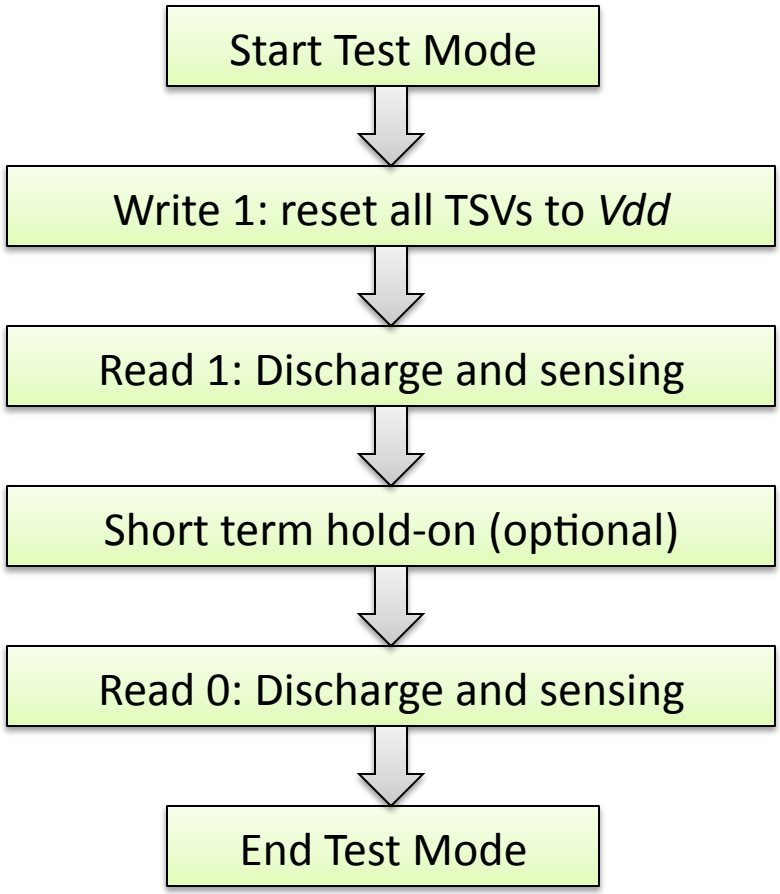
- Certain defects can alter capacitance of TSVs
  - Breaks (stuck-open or resistive)
  - Insulator defects (non-uniformity, impurity)
- Capacitance can be indirectly measured through tuned sense amplifier
- Can detect defects pre-bond, before thinning



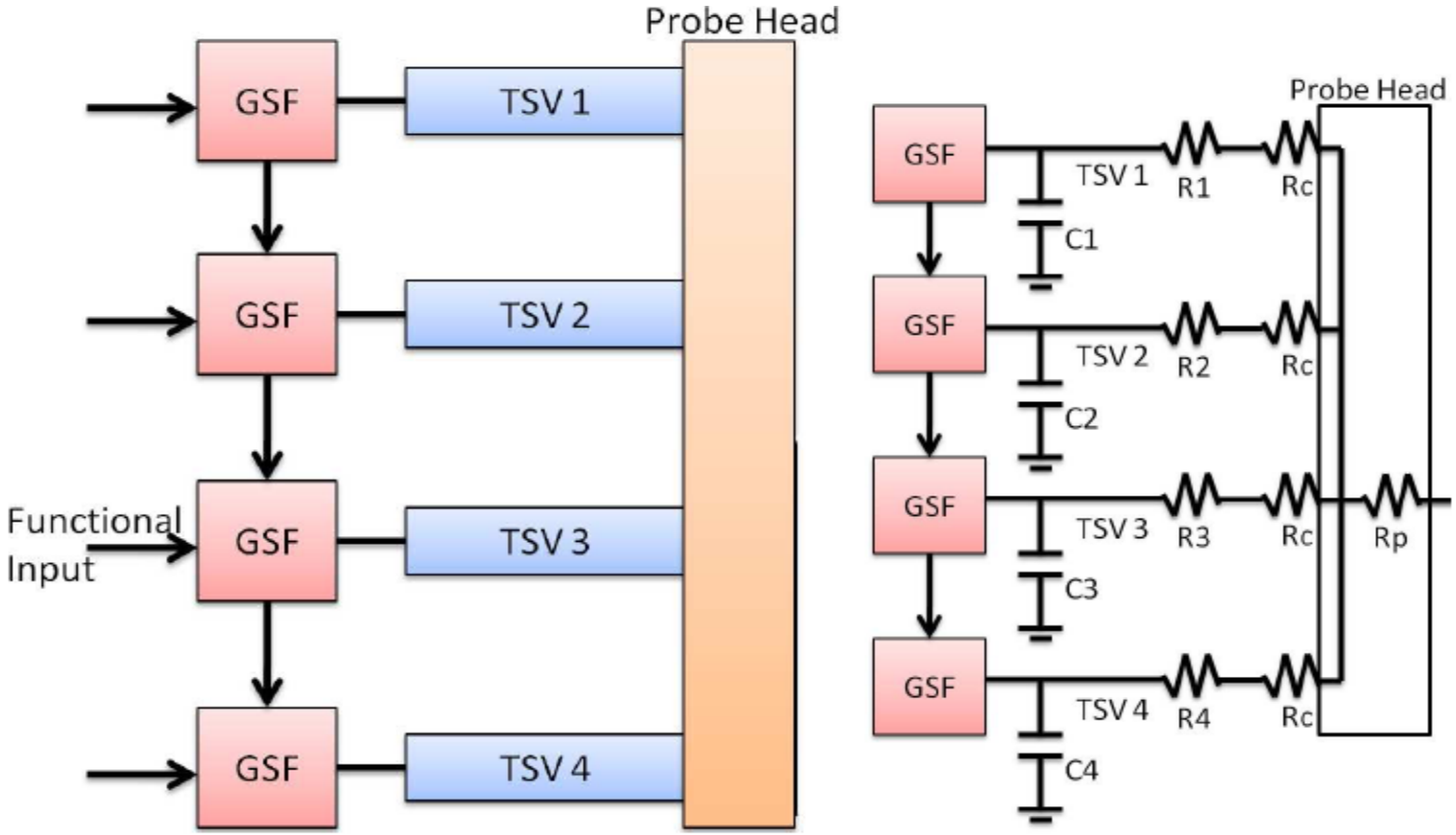


TSV Capacitance Testing
(ITRI, Taiwan)

- Determine acceptable capacitance range for TSV
- Treat each TSV as DRAM cell
- Charge TSVs, discharging and checking bounds via sense amplifier
- Factors: discharge current, discharge time, sense amplifier threshold
- Calibration? High overhead (per TSV)?



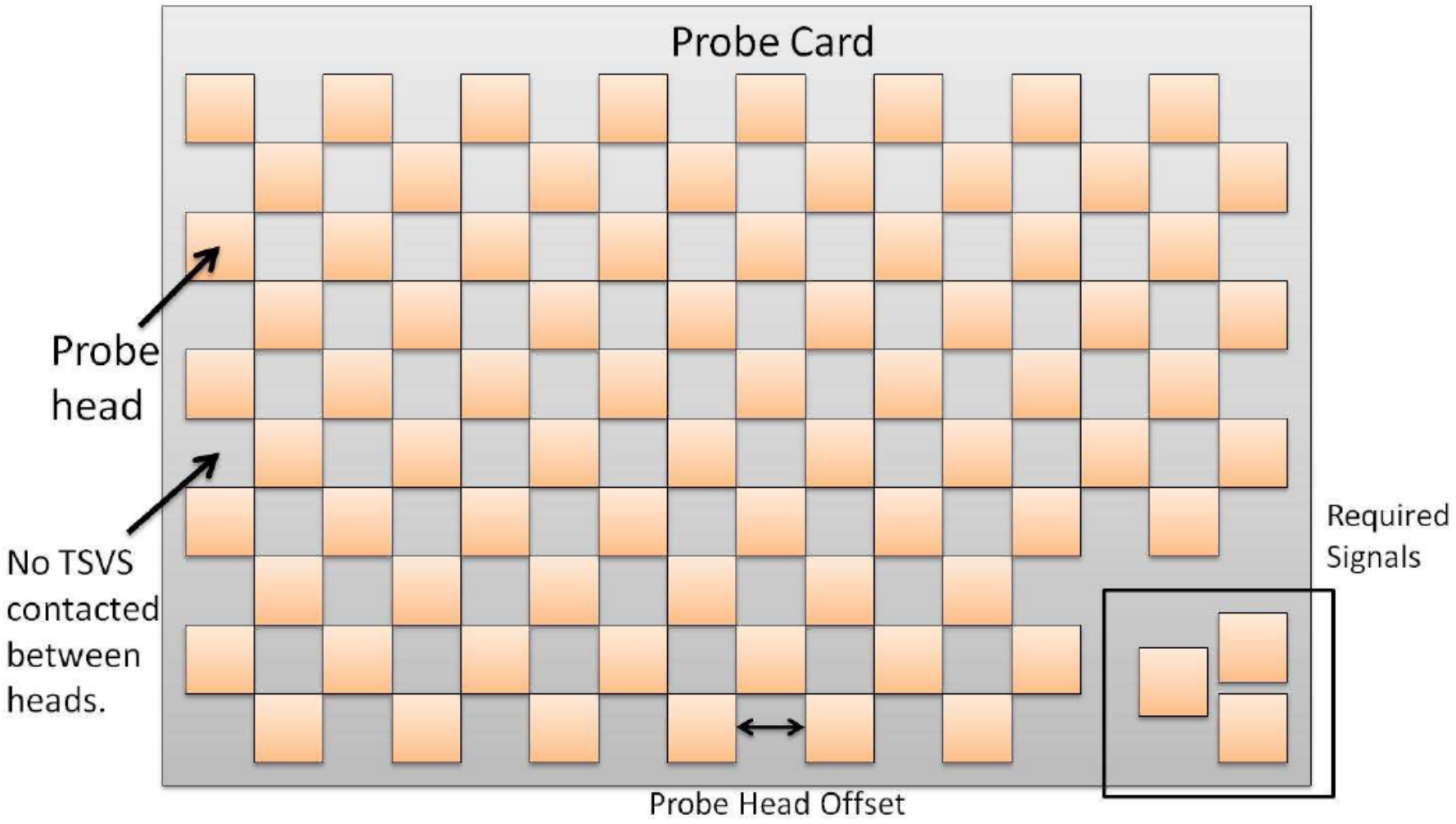
Probing “TSV Networks”



$$C_{net} = C_1 + C2 + \cdots + C_n$$

$$R_{net} = R_p + \left(\frac{1}{R_1 + R_c} + \frac{1}{R_2 + R_c} + \cdots + \frac{1}{R_n + R_c} \right)^{-1}$$

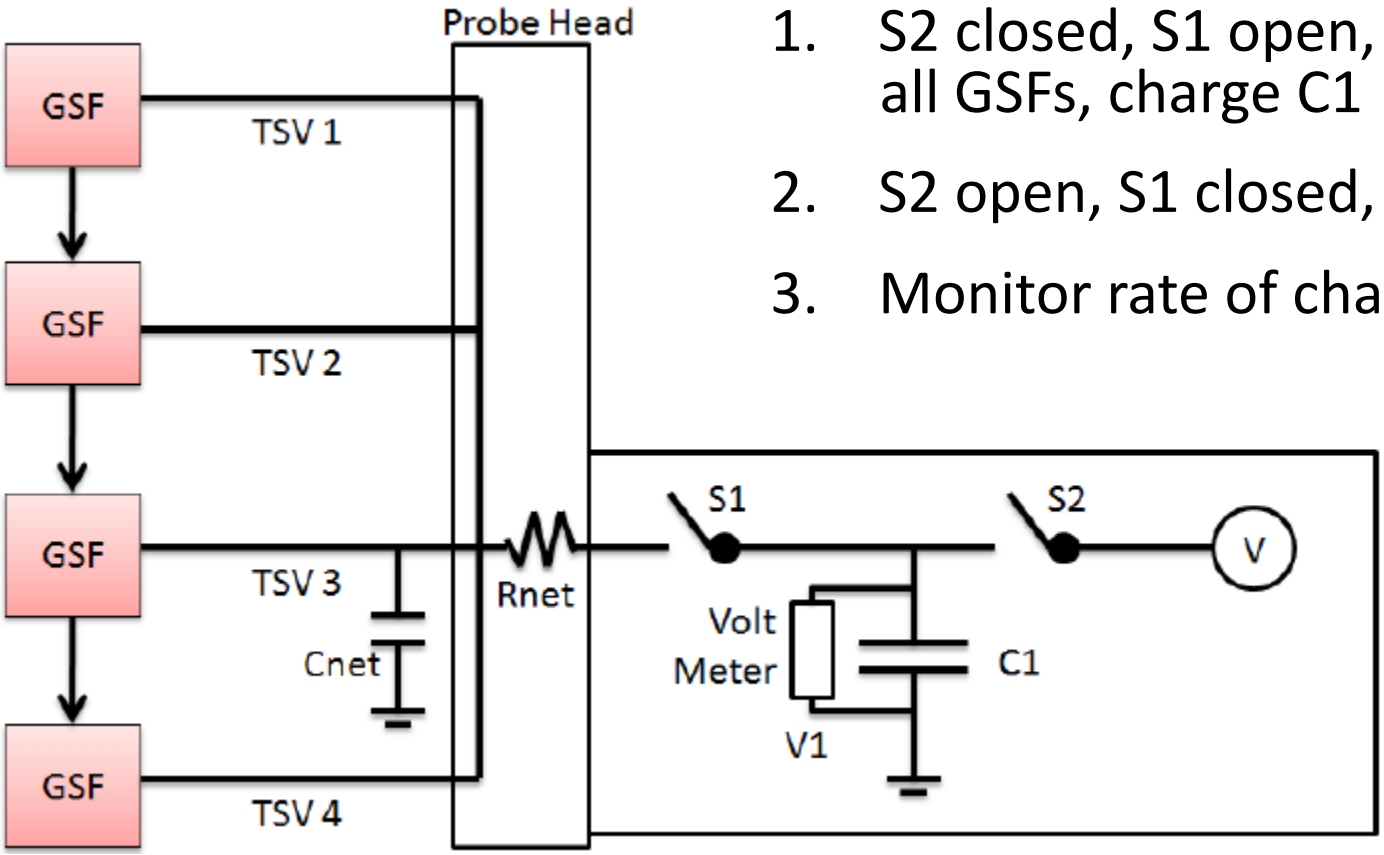
Probing TSV Networks



Probe-Head Electronics

- Charge sharing circuit
  - C1 significantly (order of magnitude) larger than expected net capacitance.
- Capacitance measurement (net), resistance measurement (per TSV)

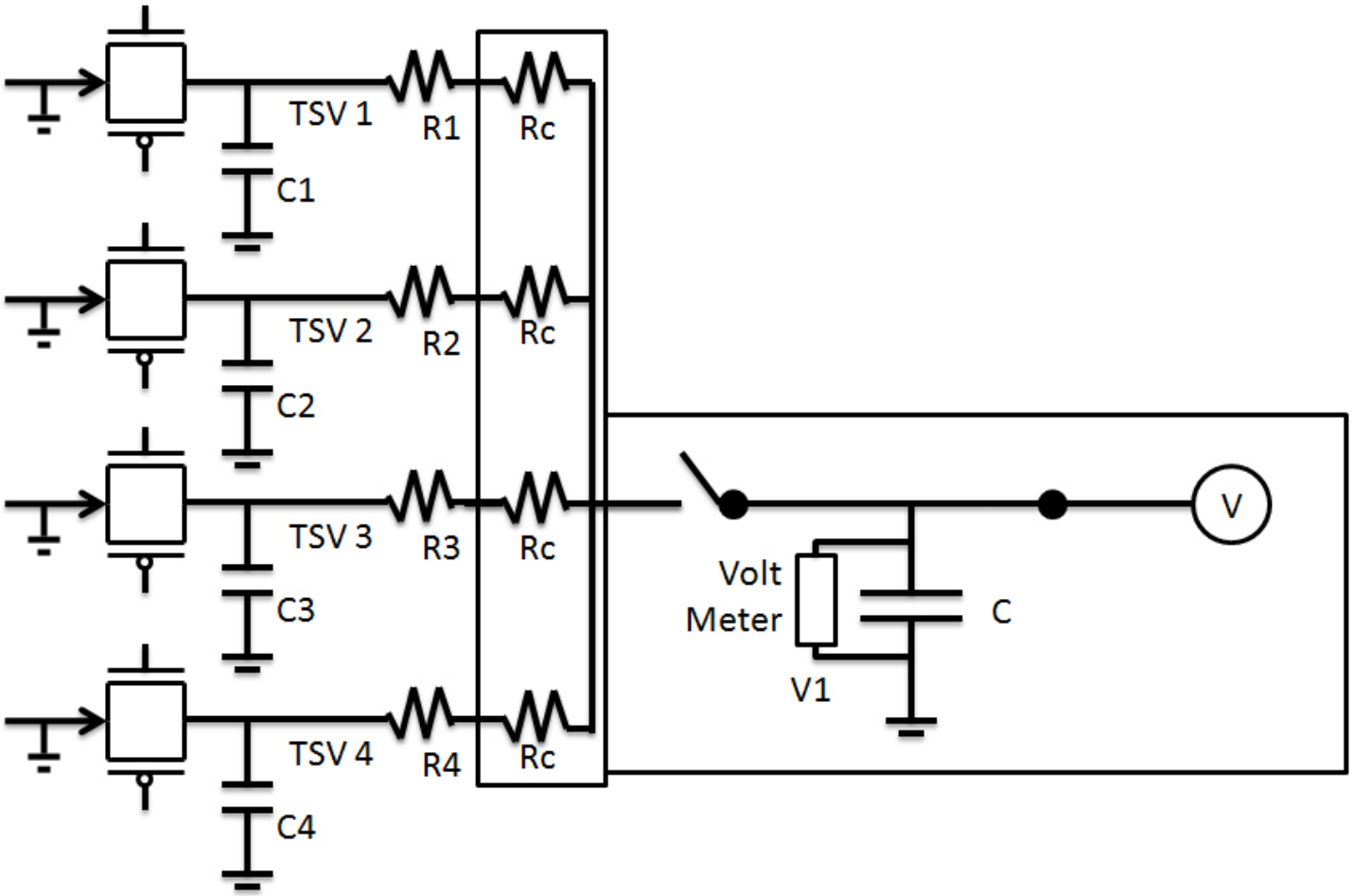
Capacitance Measurements:



1. S2 closed, S1 open, 0 loaded to all GSFs, charge C1
2. S2 open, S1 closed, discharge C1
3. Monitor rate of change of V1

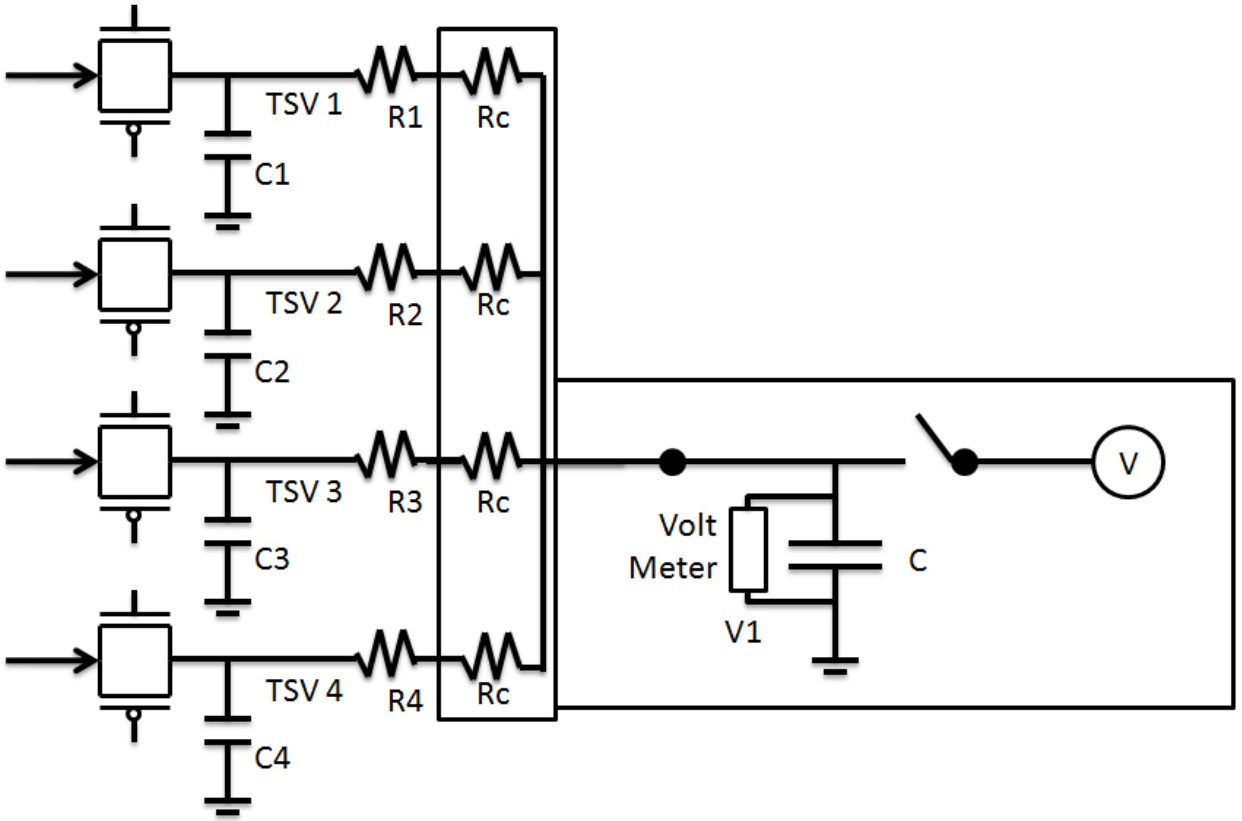
Capacitance Measurements

1. S2 closed, S1 open, 0 loaded to all GSFs, GSFs closed



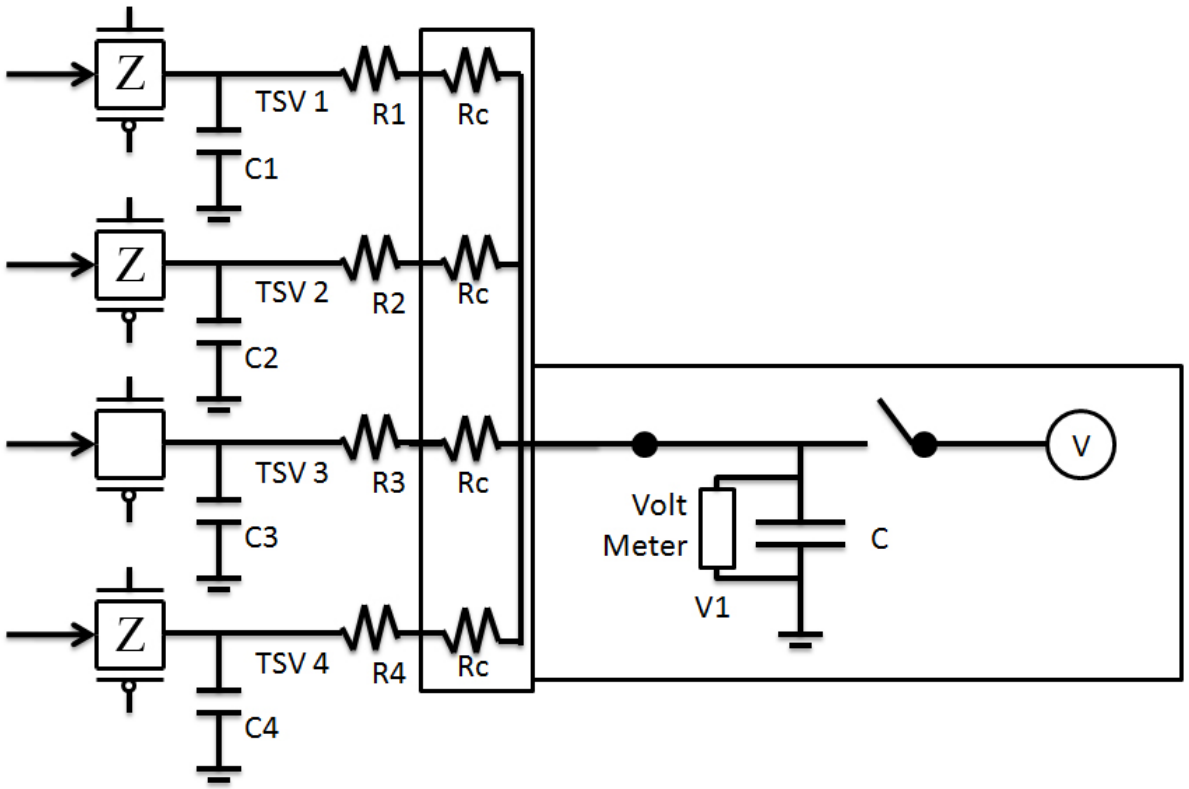
Capacitance Measurements

2. S2 open, S1 closed, GSFs open
3. Monitor rate of change of V1



Resistance Measurements

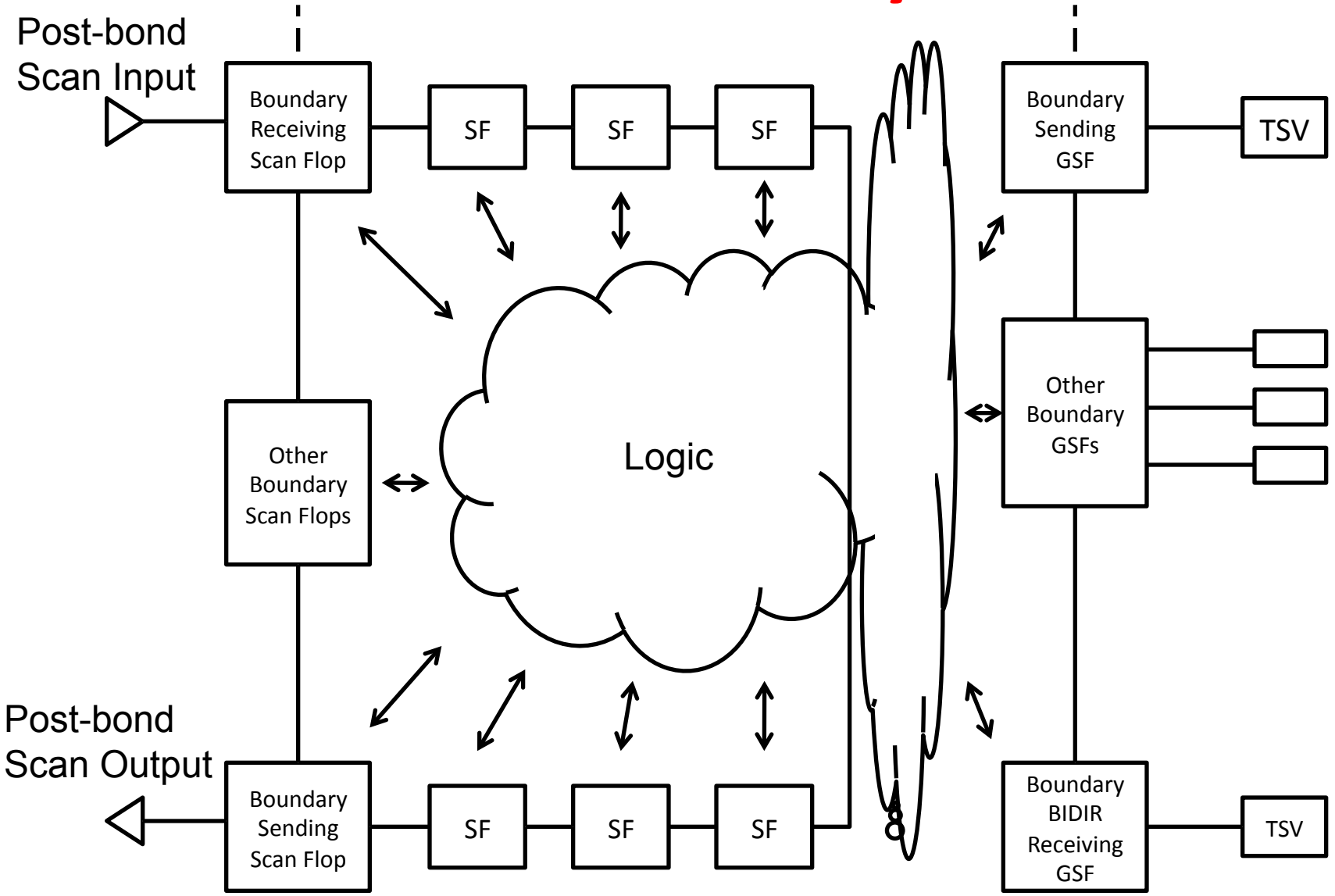
1. Discharge C, TSV network.
2. 1 loaded to all GSF, S2 open, S1 closed.
3. Open one or more GSF, charge C to threshold, measure charge time.



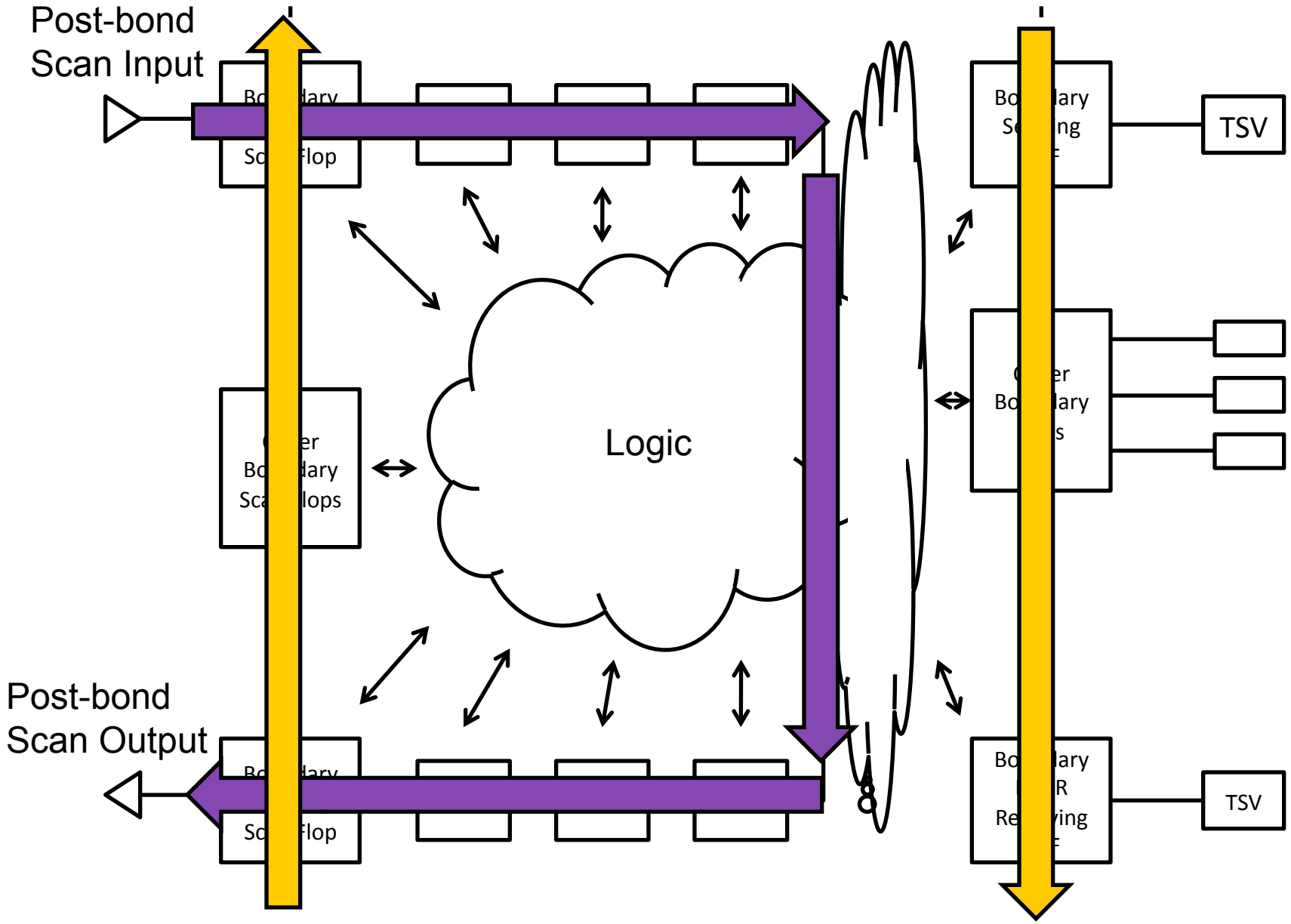
Pre-Bond Scan Test

- How to test the die logic?
- Reconfigurable scan chains: enable pre-bond scan test of die logic through TSV networks
  - Post-bond configuration: test data enters/exits die through interface with lower dies in stack or external test pins
  - Pre-bond configuration – Boundary GSFs become new scan chain I/O
  - Multiplexers: switch between scan chain modes

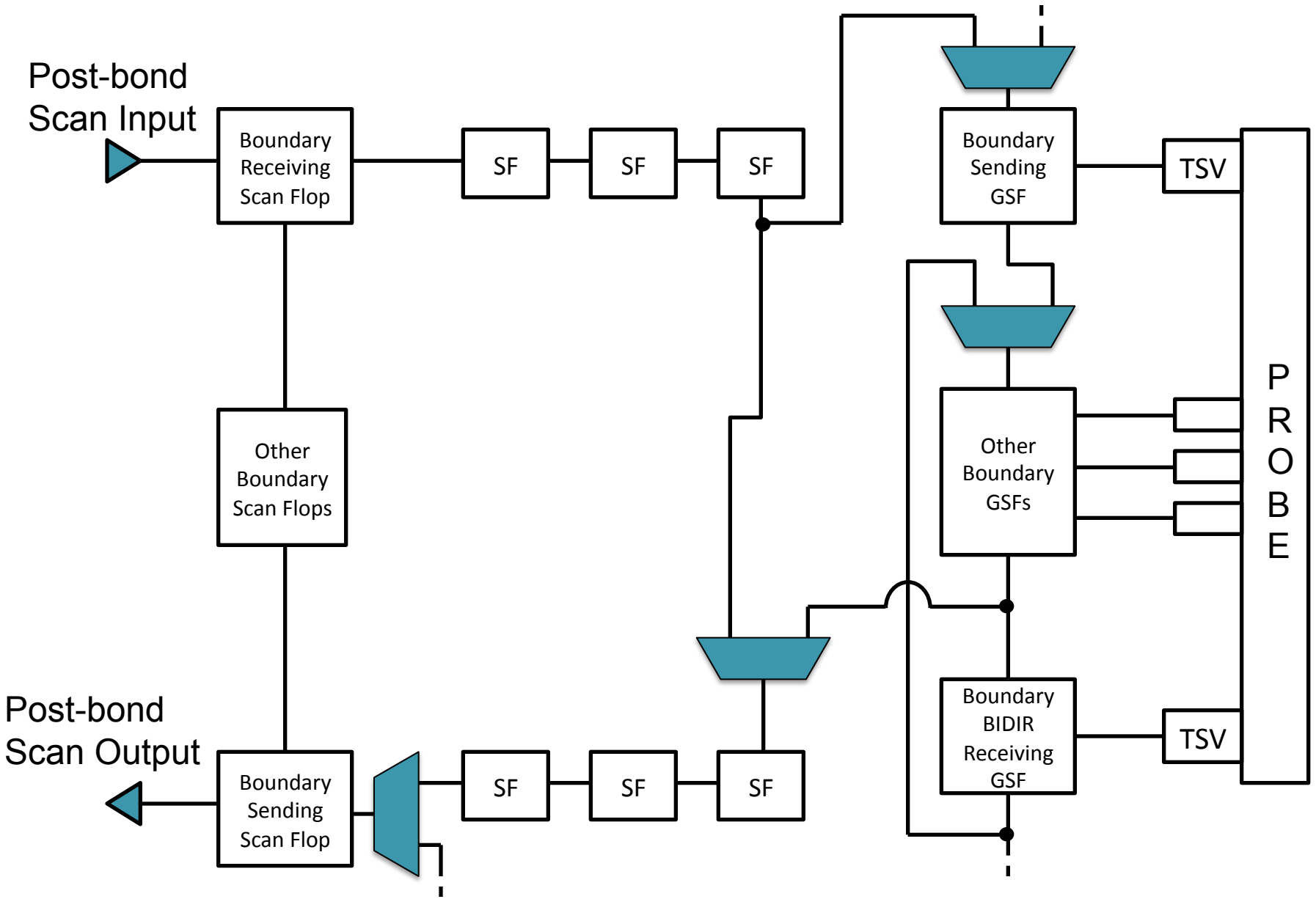
Internal and Die Boundary Scan Chains



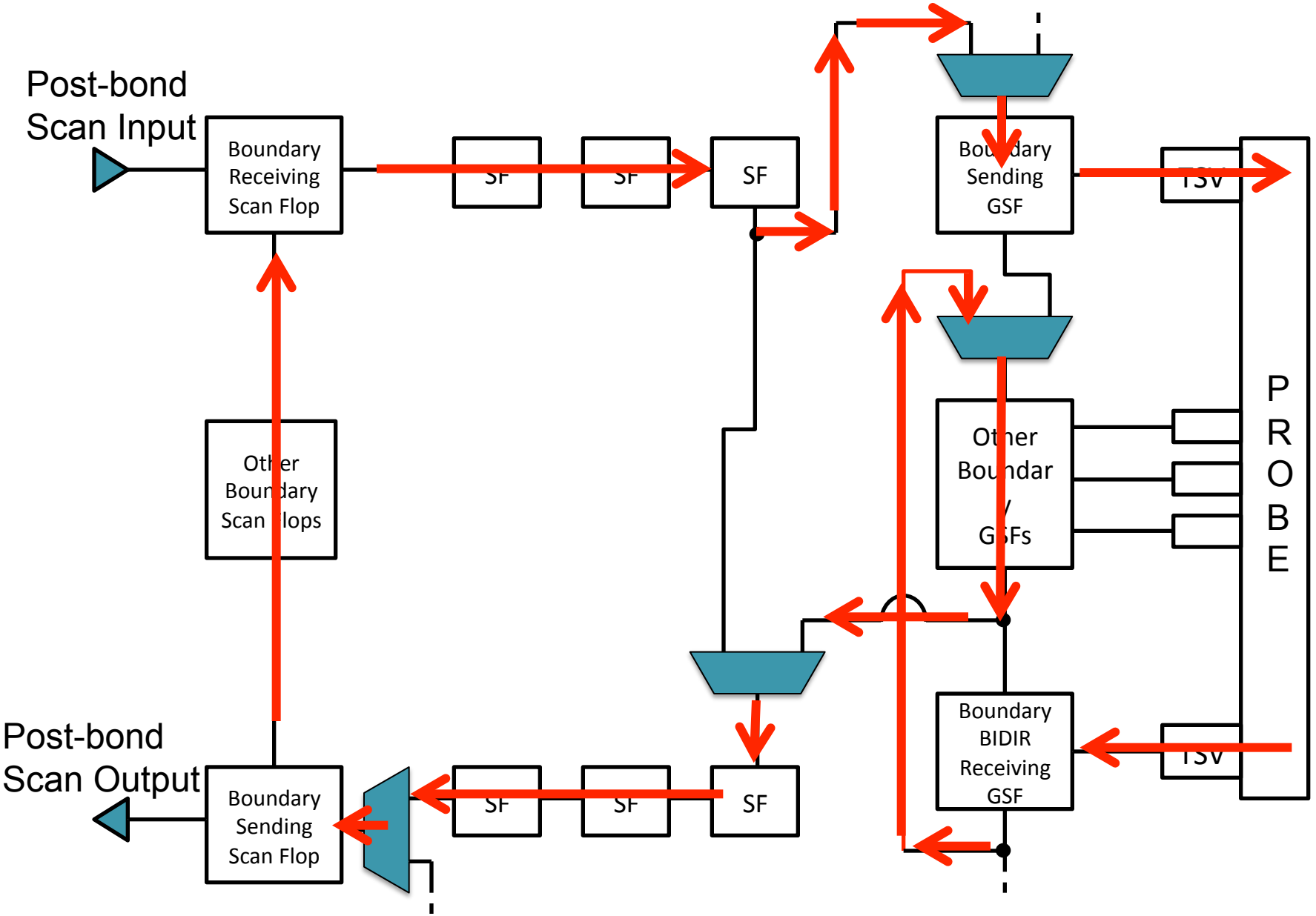
Post-Bond Test Data



Scan Chain Reconfiguration Muxes



Pre-Bond Test Data



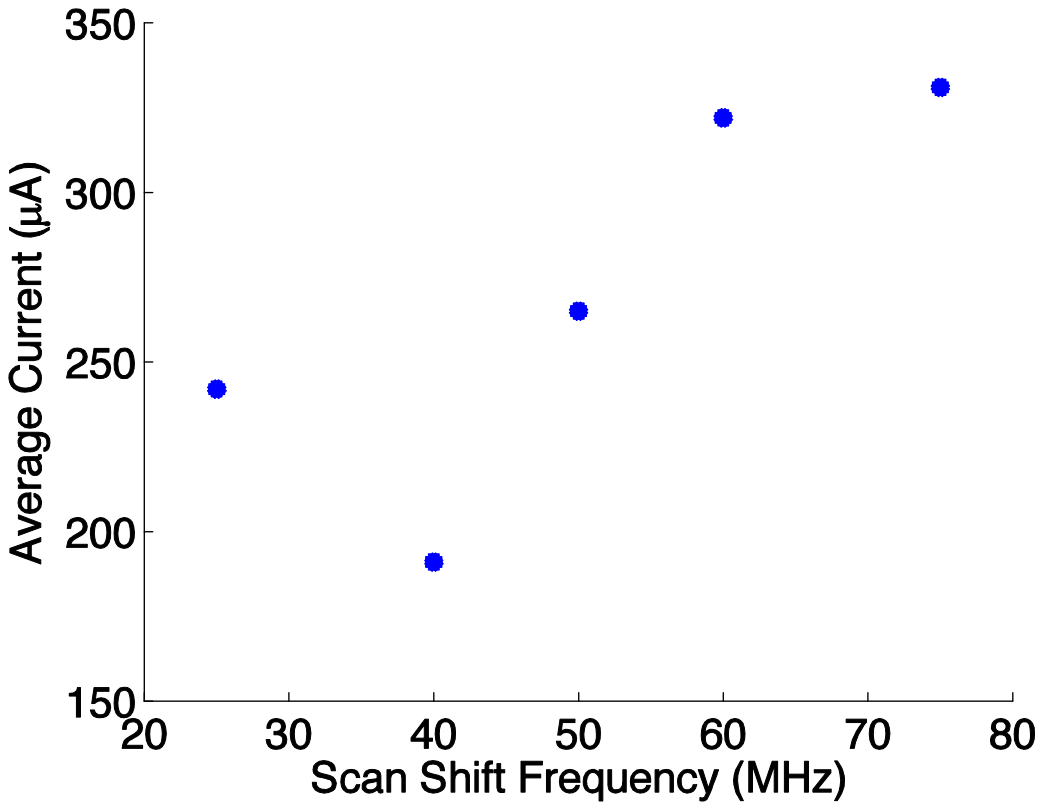
Feasibility Considerations

- Must provide current necessary for scan test through TSVs
- Relatively high TSV network capacitance must not significantly increase test time
- Area overhead of proposed method must be small
- Boundary scan registers needed for high pre-bond fault coverage?

Evaluation: Benchmark Circuit

- Fast Fourier Transform circuit from OpenCores benchmarks split between 4 dies
  - 45nm technology
  - 299,273 gates and 19,962 flops
  - 463 to 936 TSVs between dies
  - 5 µm TSV diameter
- Stuck-at fault coverage as low as 44.76% without boundary registers, as high as 99.97% with
- Boundary GSFs and reconfiguration circuitry: 2.2% of total number of gates

Average Current (Hspice Simulations)



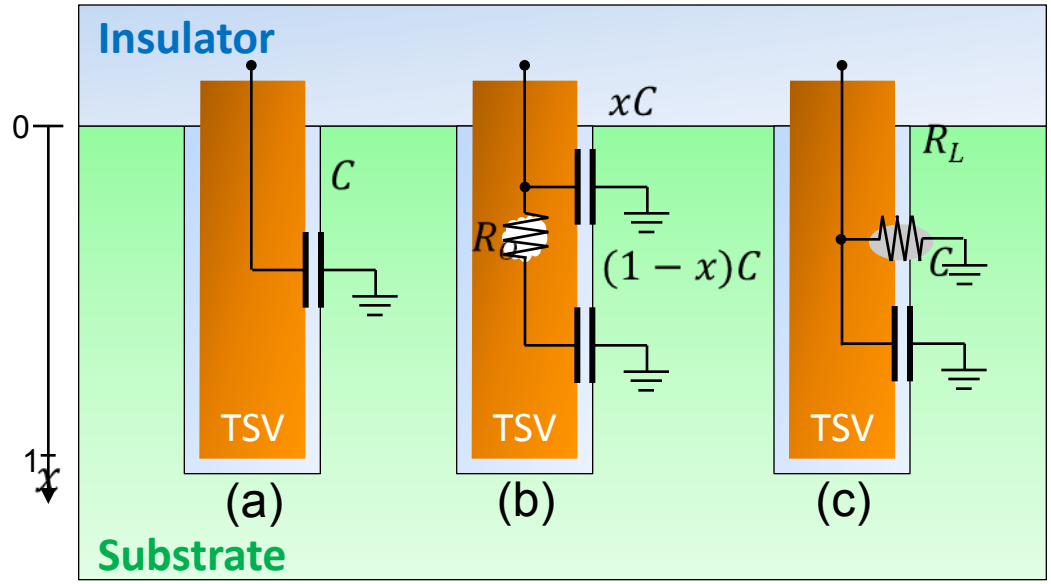
- Avg. current of 300 µA corresponds to density of 1528 A/cm^2
- TSVs reliable with sustained current density of 15,000 A/cm^2

Peak Current

Test Parameter	Die 0	Die 1	Die 2
Peak Current	1 mA	1 mA	1.1 mA
Avg. Current (Stuck-at)	300 µA	294µA	327µA
Avg. Current (Transition)	432 µA	341µA	383µA
Area Overhead	2.2 %	1.0 %	1.2 %

- Cantilever probe tip capable of supplying 3 A of current
  - Upper limit on instantaneous current drawn assuming peak current in all scan chains simultaneously

Non-Invastive Pre-Bond TSV Test: TSV Fault Modeling



$C = 60$ fF
$R_O = 0 \ldots 3$ kΩ
$R_L = 0 \ldots 10$ kΩ

a) Fault-free case: lumped capacitor $C = 60$ fF
($R_{TSV} < 1$ Ω → neglect R_{TSV})

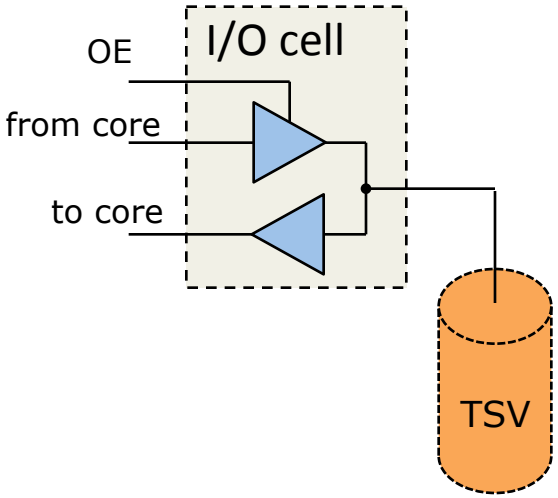
b) Resistive open fault: $R_O = 0 \ldots 3$ kΩ at the location x

c) Leakage fault: $R_L = 0 \ldots 10$ kΩ

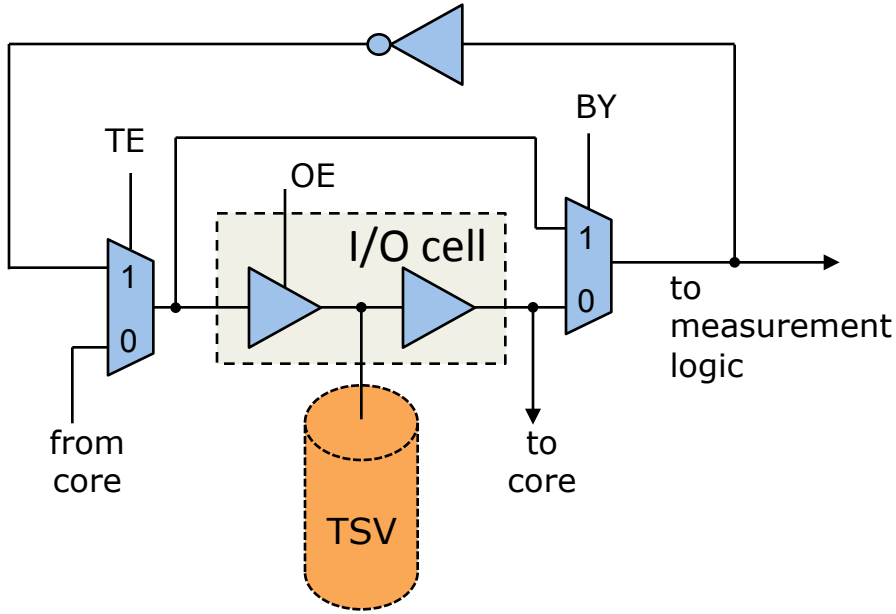
Main idea: parametric test for R_O and R_L

Ring Oscillator Configuration

Functional circuitry:



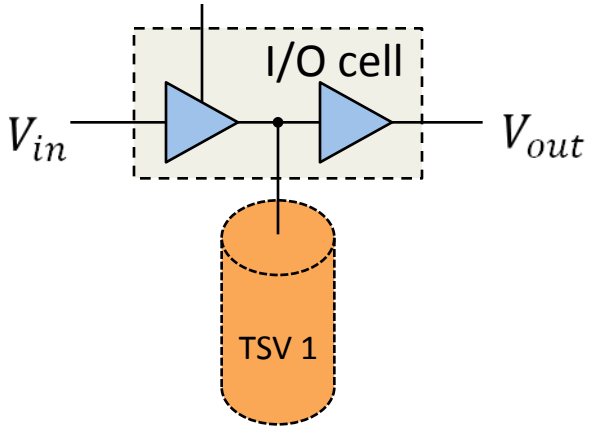
Design-for-Test extension:

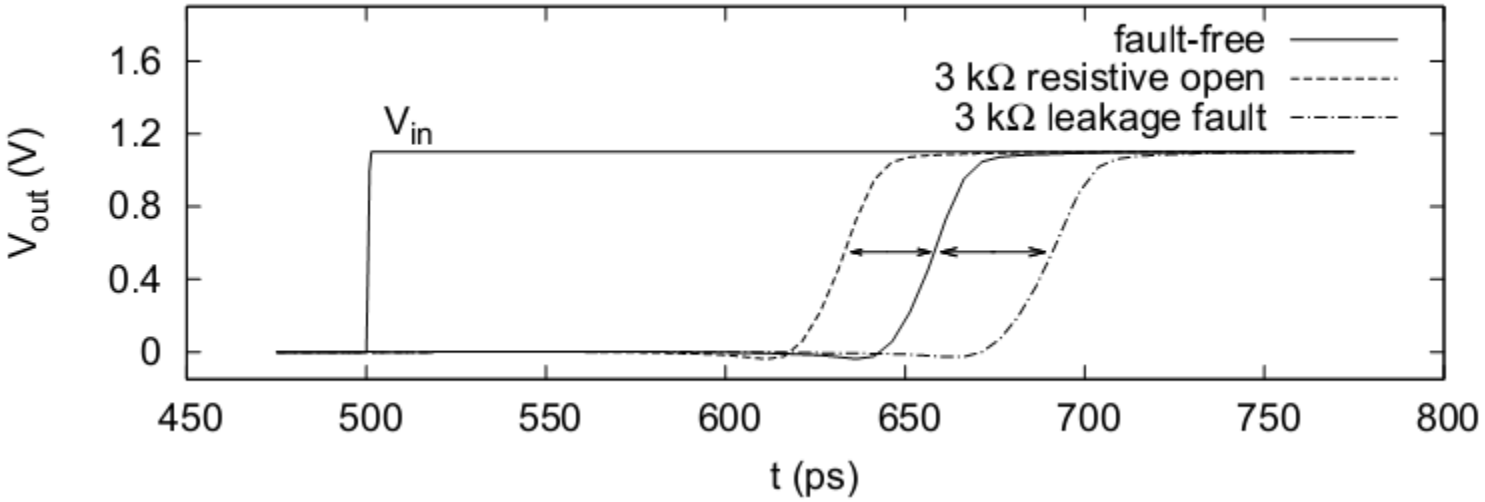


- Assumption: bidir I/O cells
- Create ring oscillator using I/O cell and inverter
- Use TSV as capacitive load
- TE selects between functional and test operations
- BY selects between the TSV under test and bypass path

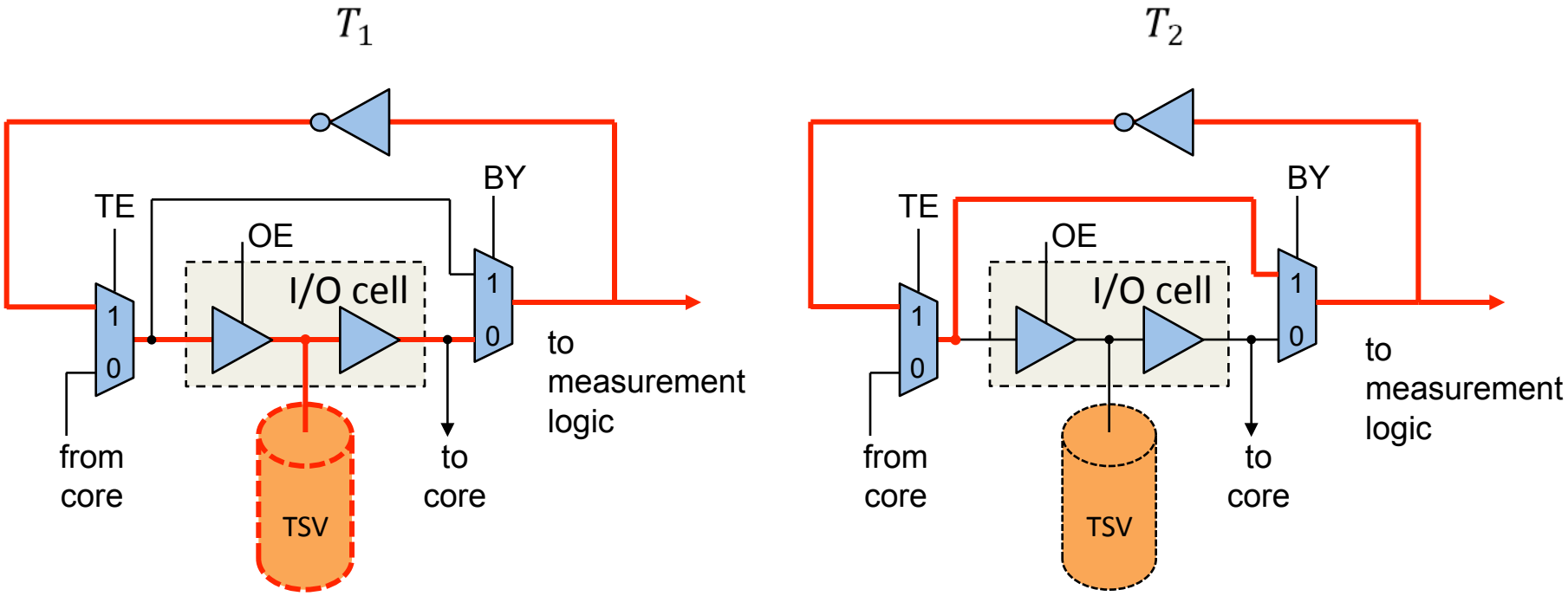
Determine R_f and R_0 by measuring oscillation period

Difference in Propagation Delay



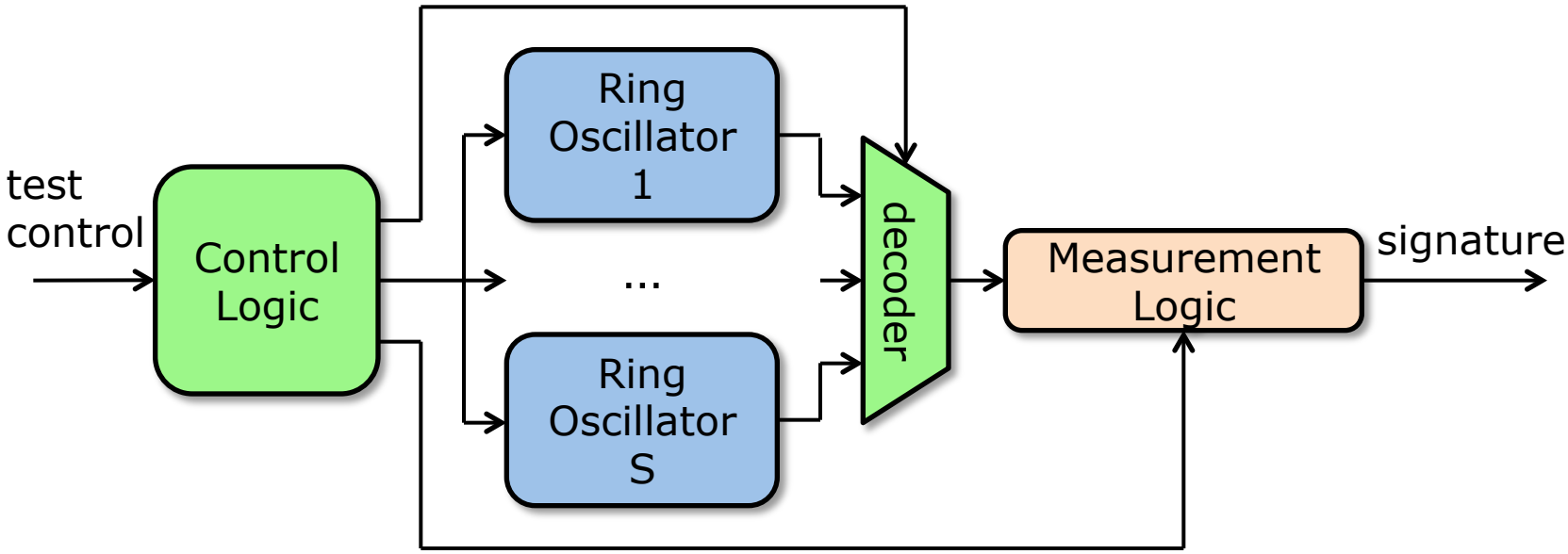


Ring Oscillator Configuration



- Measure difference $\Delta T = T_1 - T_2$ to reduce inaccuracy due to random process variations
- ΔT sensitive to defects in TSVs
  - ΔT⬇ if resistive open
  - ΔT⬆ if leakage

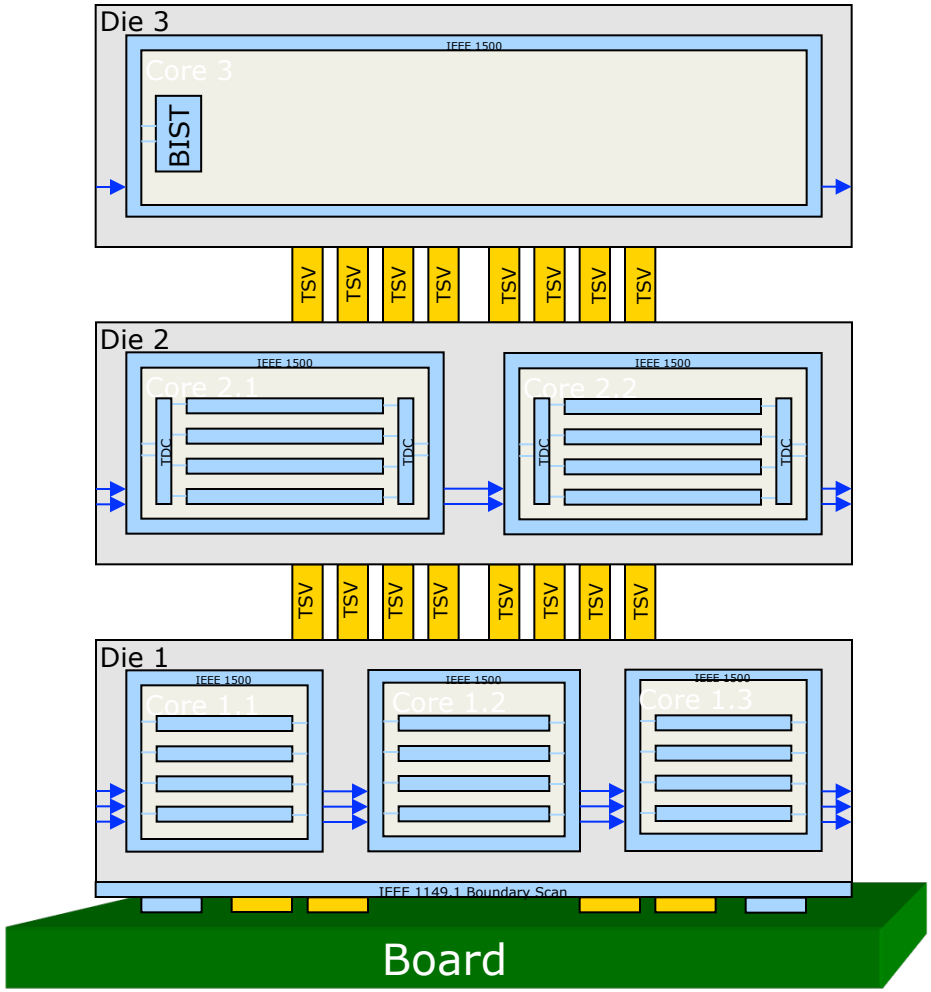
Overall Architecture



- S ring oscillators share one measurement logic
  + less area overhead
  − sequantial test
- Measurement logic:
  - Binary counter
  - LFSR

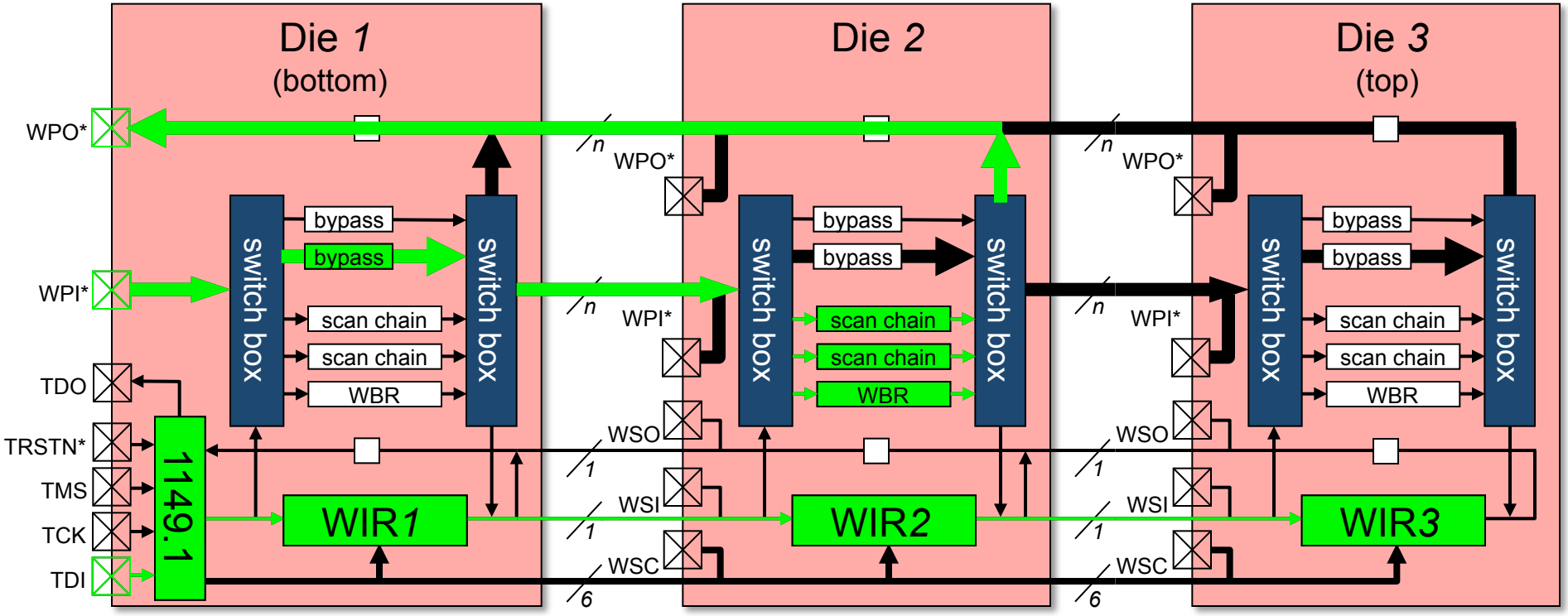
Stack (Post-Bond) Testing: Test Delivery and DFT Hierarchy

- Core-level DFT
  - Scan chains, Compression, BIST
- Die-level DFT
  - Wrappers and test-access mechanisms (TAMs)
- SIC-level DFT
  - Wrapper at die boundary
  - KGD: Extra probe pads
  - KFS: Test Elevators
  - Switches
  - Board-level DFT (IEEE 1149.1)



Reconfiguration During TestTime

Test set-up example: **Intest** of **Die 2** using **parallel TAM**



ParallelPostbond
BypassElevator

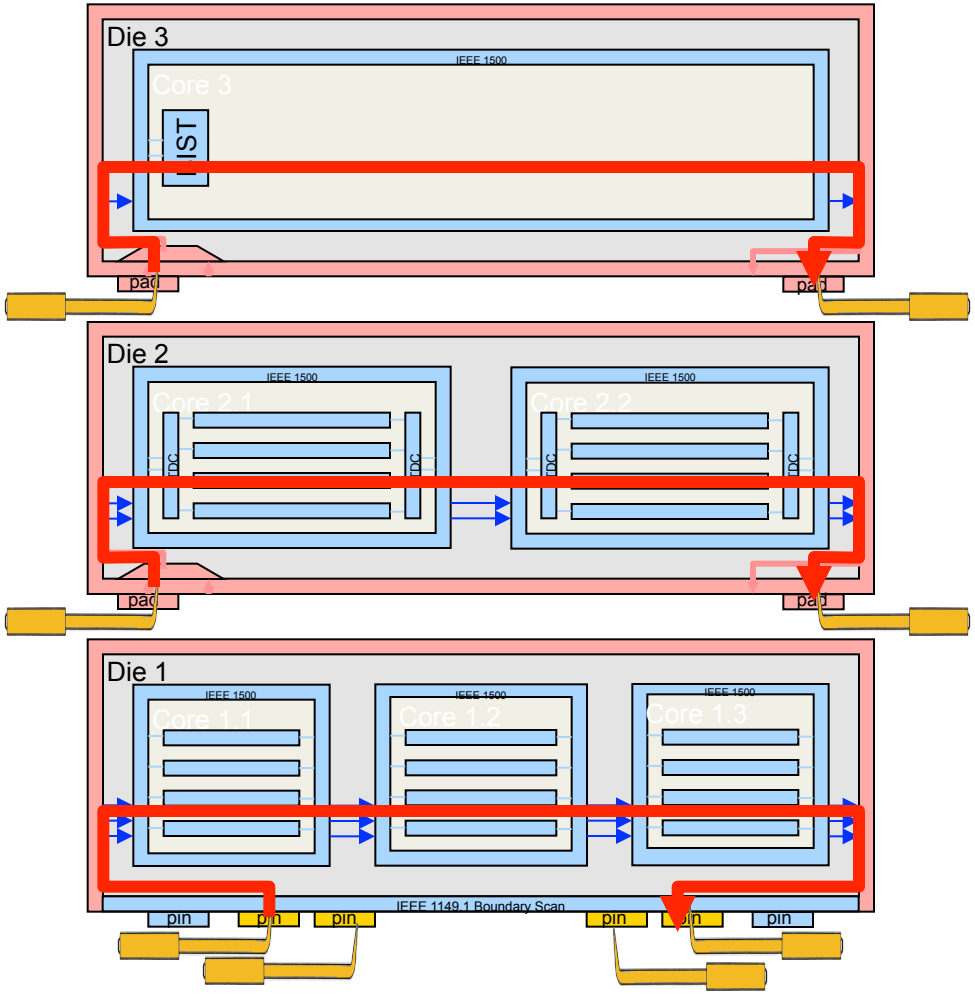
ParallelPostbond
IntestTurn

ParallelPostbond
BypassTurn

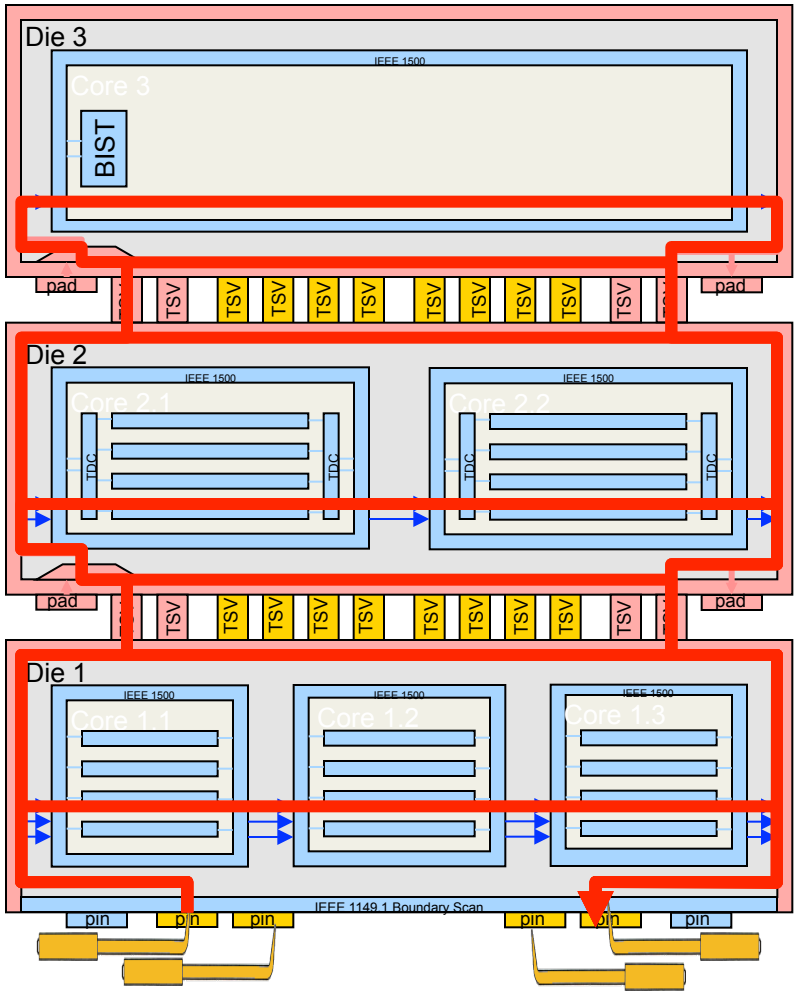
3D DfT Architecture – Overview

(IEEE P1838)

Pre-Bond Testing

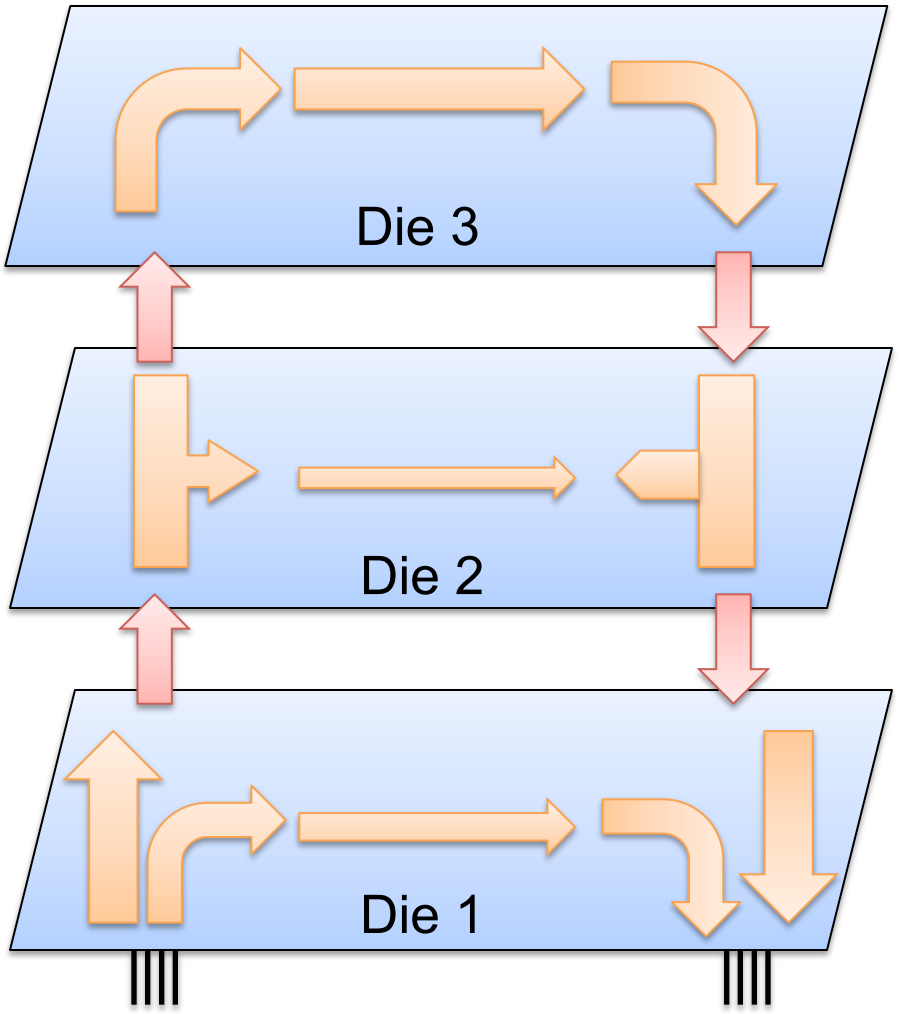


Post-Bond Testing



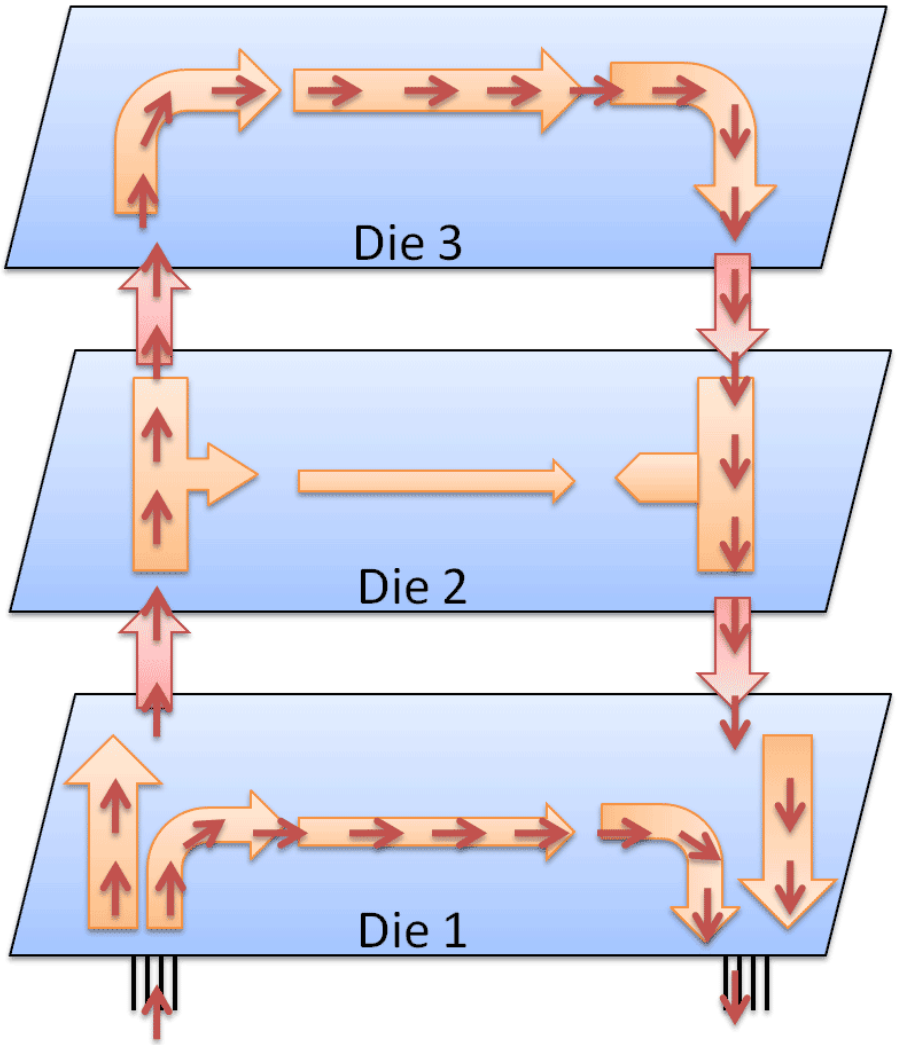
DFT: Post-Bond Testing Considerations

- Serial/parallel testing of die
  - How many dedicated test TSVs to use?
  - How to maximize test pin utilization?
  - What test schedule should be followed?
- Optimization of die testing architecture
  - How wide should each die TAM be?



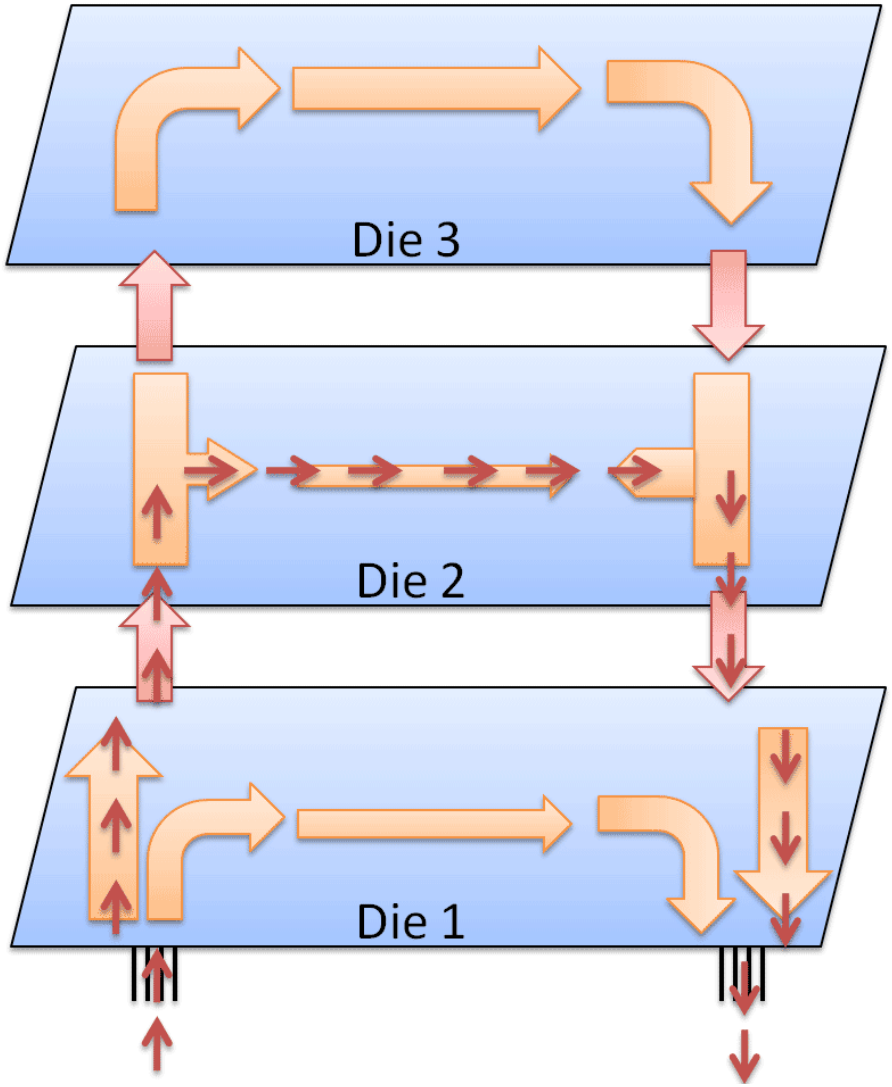
DFT: Post-Bond Test Considerations

- Example: Die 1 and Die 3 tested in parallel…
  - Test data enters and exits stack through test pins on bottom die
  - On-die DFT architecture routes test data to/from die-internal TAM
  - TestElevators send test data up and down the stack

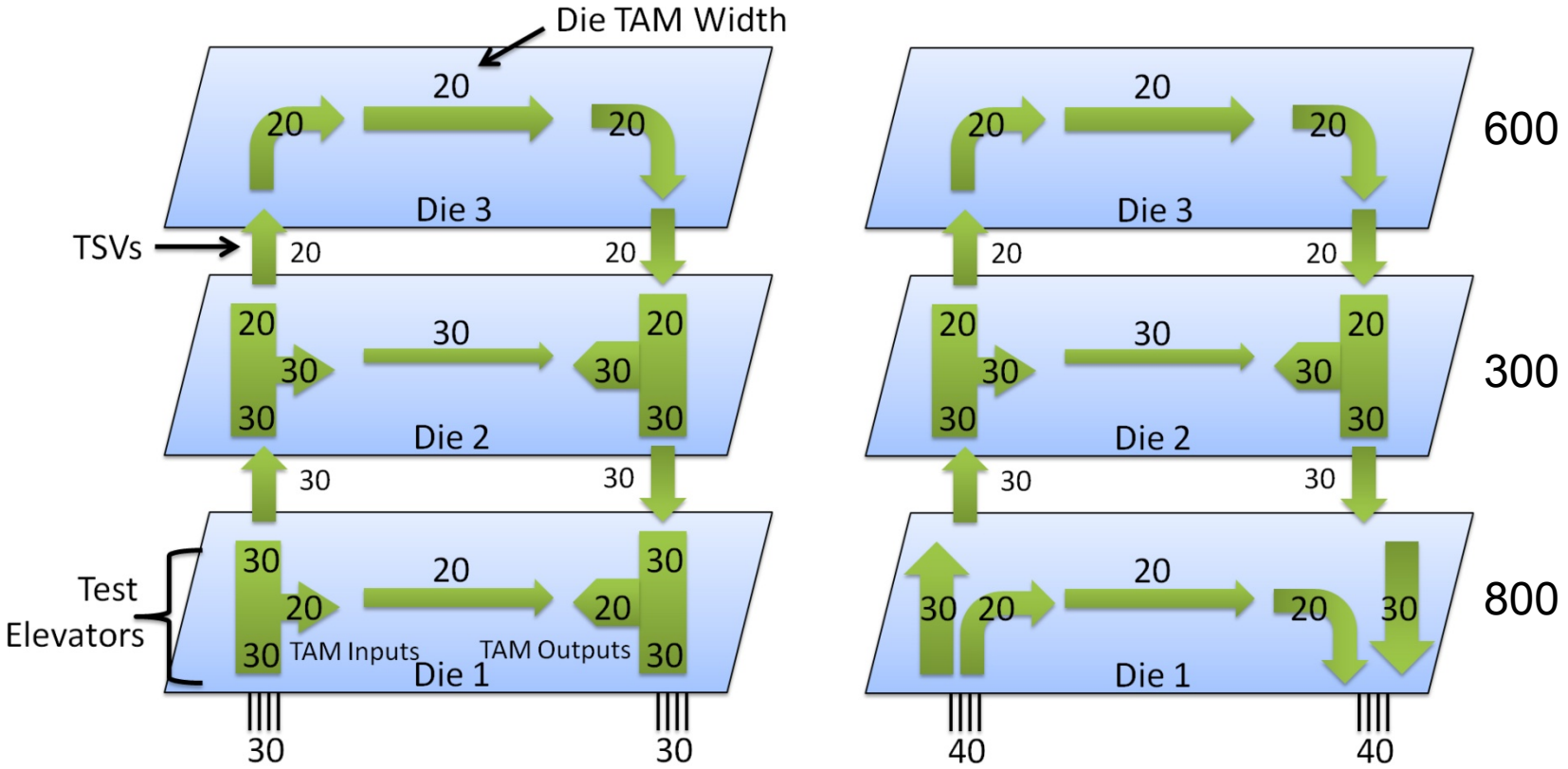


DFT: Post-Bond Test Considerations

- …followed by testing of Die 2
- Tradeoffs:
  - Generally, more test pins required for parallel testing
  - Generally, more TSVs required for parallel testing
  - Parallel testing reduces test time



Optimization for Final Stack Test

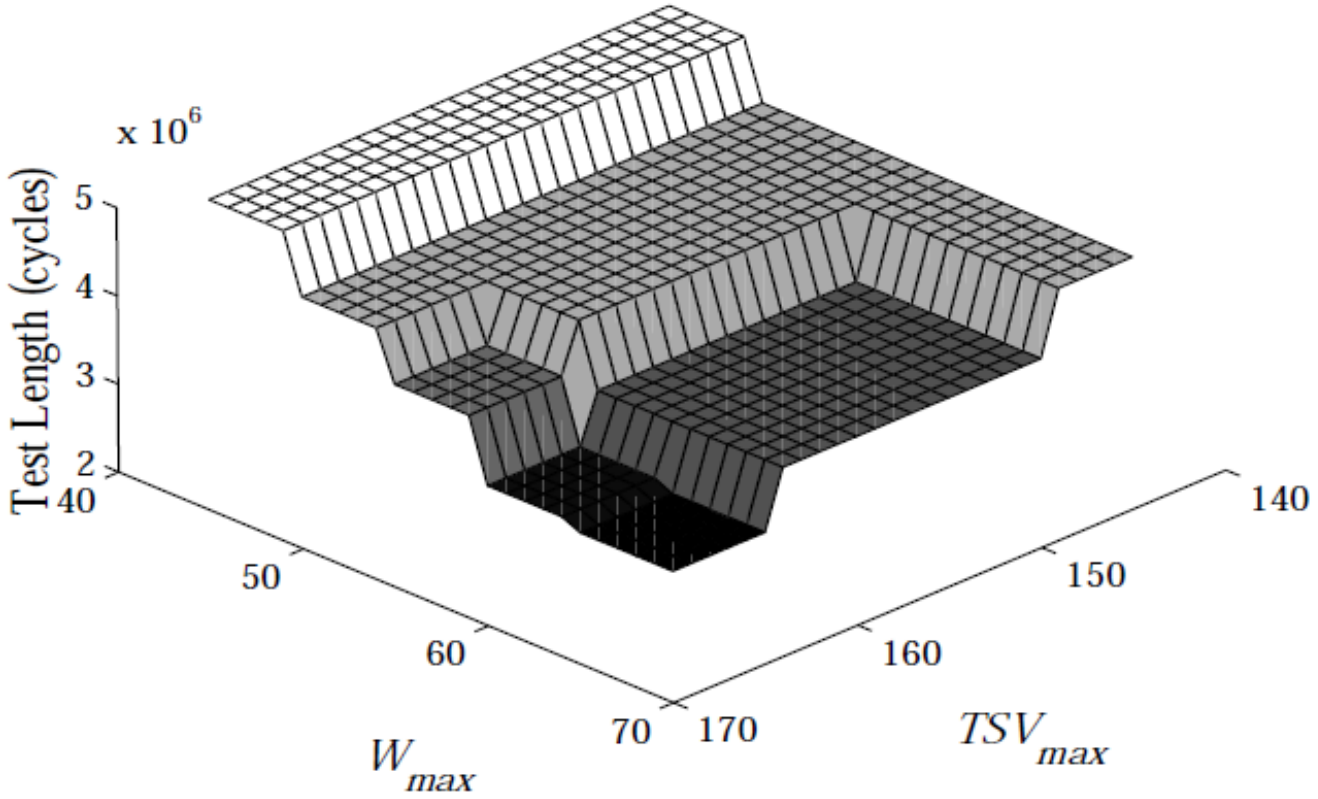


- Left: All die tested serially, test time: 1700 cycles
- Right: Die 1 and 3 tested in parallel, test time: 1100 cycles
- Challenge: How to systematically and quickly search the space of 3D TAM and test scheduling solutions?

Test-Time Optimization

- Integer linear programming (ILP)
- Minimize test time (Objective function)
- Constraints: System of linear constraints
  - Limits on no. of package pins, no. of test elevators, whether dies are tested in series or in parallel,…
- A solution to the ILP model provides:
  - Minimum test time
  - Optimal 3D test architecture
  - Optimal test schedule
- Problem instances are small enough to be tackled using ILP (exact optimization)

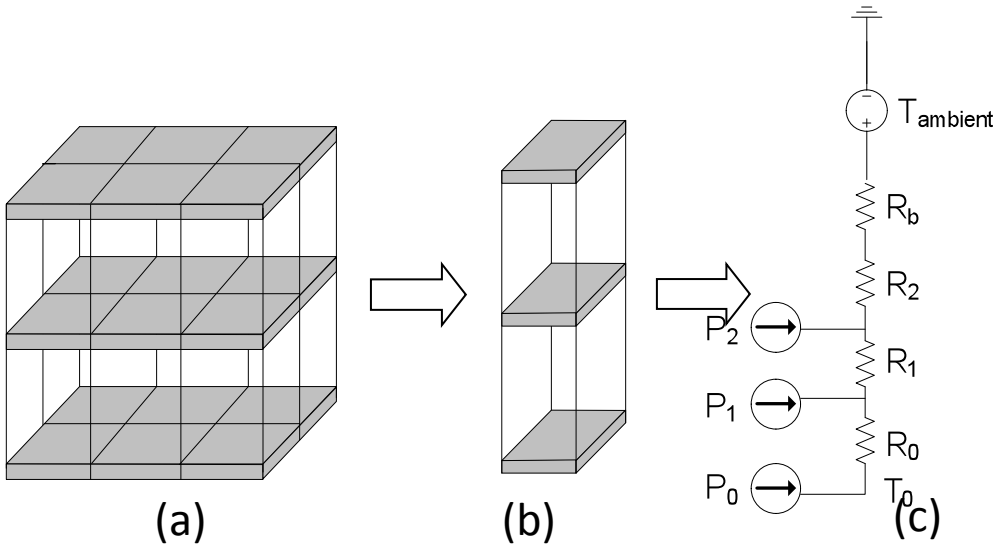
Typical-Case Result: Complete Stack Test

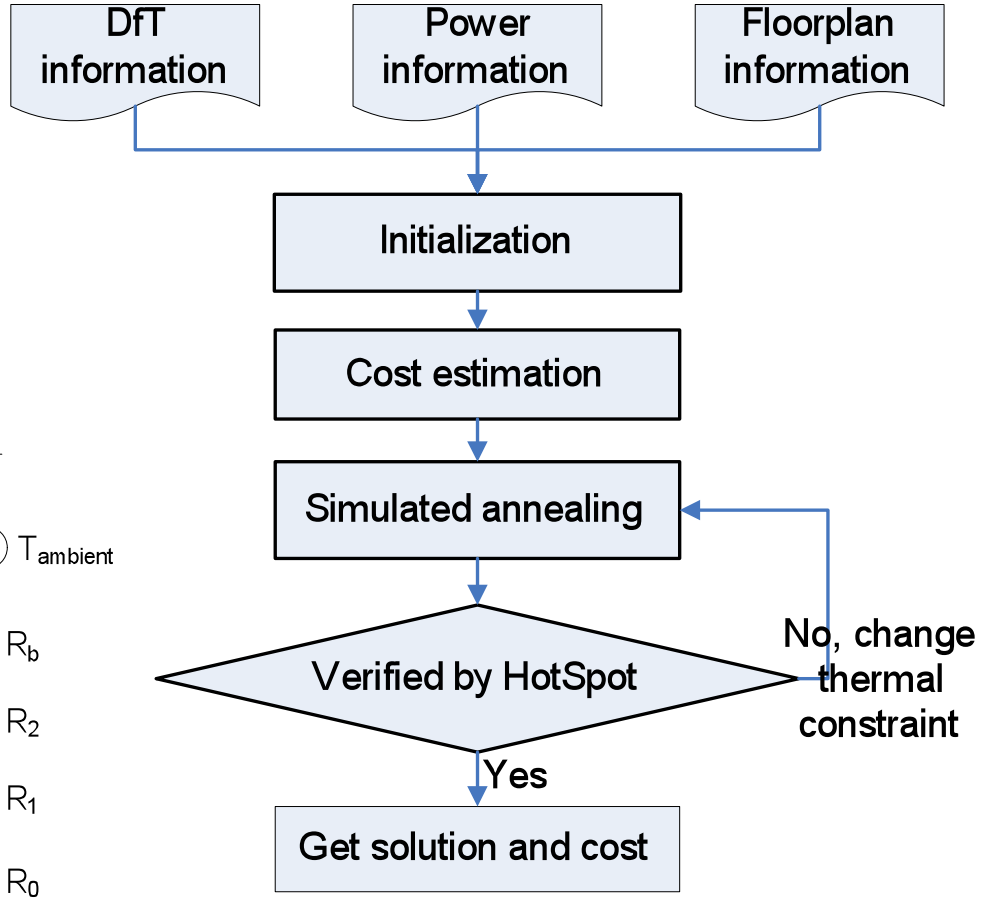


- Extra test pins provide more pay-off than extra TSVs, but they can be used together for best results

Thermal-Aware Test Scheduling

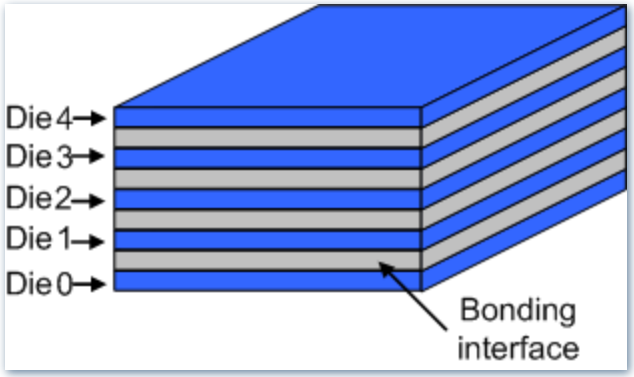
- Compute a test schedule to:
  - Minimize total test time
  - Optimize 3D TAM Under thermal constraints
- Temperature estimation, Simulated annealing





Results

- Test case
  - 5-layer 3D IC, bonding interface
  - Ambient resistance : 4 ℃/W
  - Ambient temperature : 25℃
  - Temperature limit : 90℃



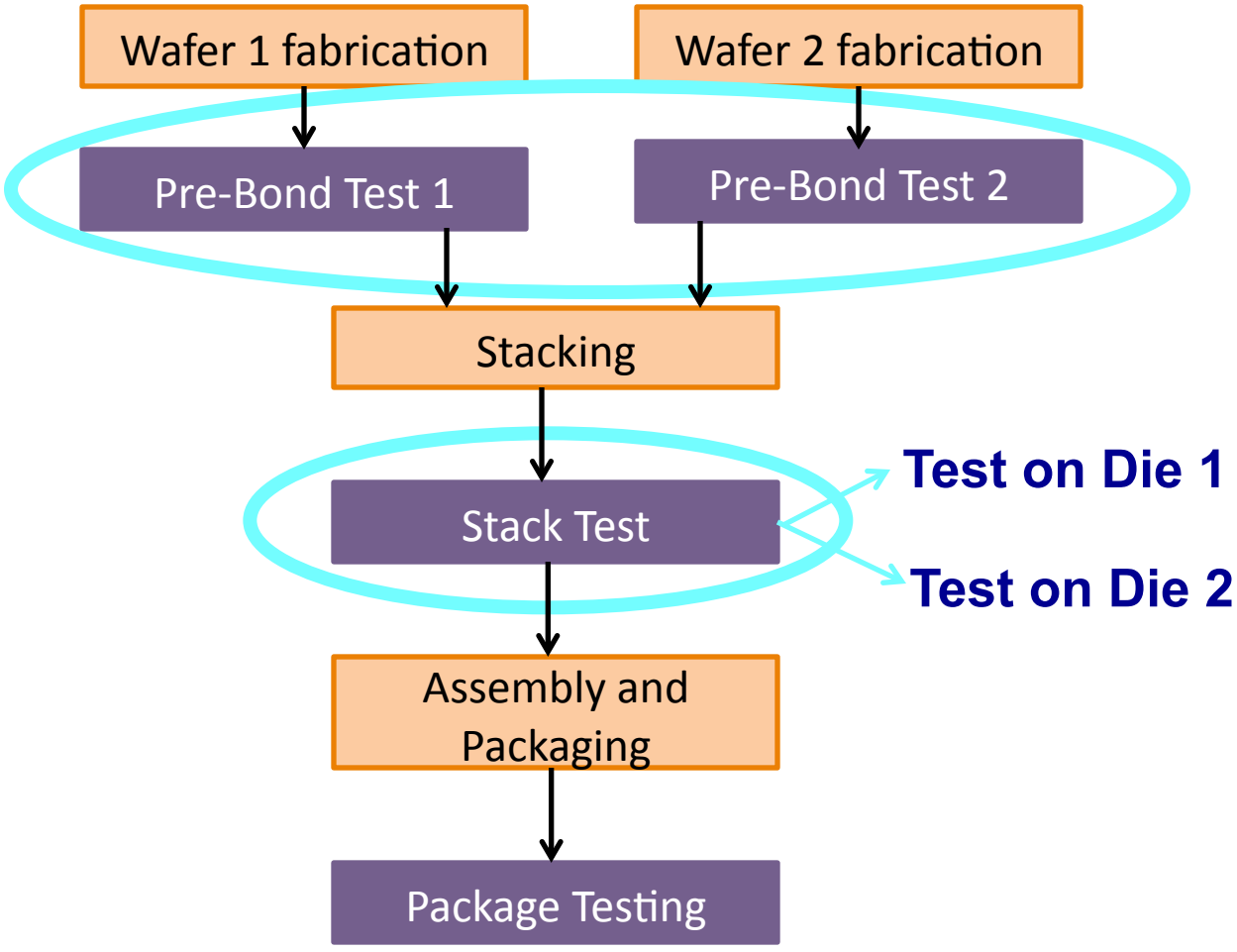
	Area (mm x mm)	Thickness (μm)	Thermal Resistivity (k*m/W)
Die	5 x 5	50	0.01
Bonding interface	5 x 5	2	0.25

TAM limit (bit)	W/O thermal limit		With thermal limit		Test time overhead
	Test length (cycle)	Max temperature (℃)	Test length (cycle)	Max temperature (℃)	
140	74,015,156	258.78	87,959,252	89.70	18.84%

Hotspot (℃)	Proposed (℃)	Error
88.50	89.70	1.36%

Test Insertions

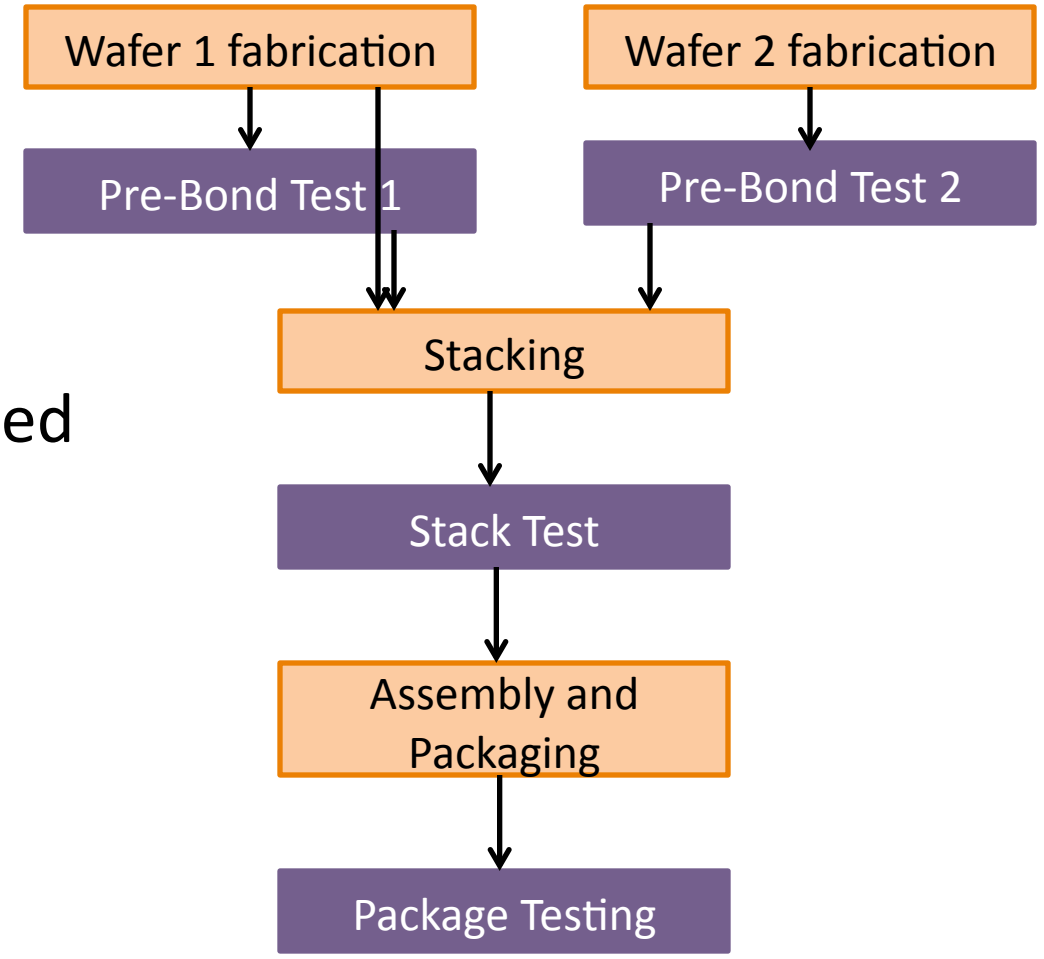
- 2-die stack



4 test insertions

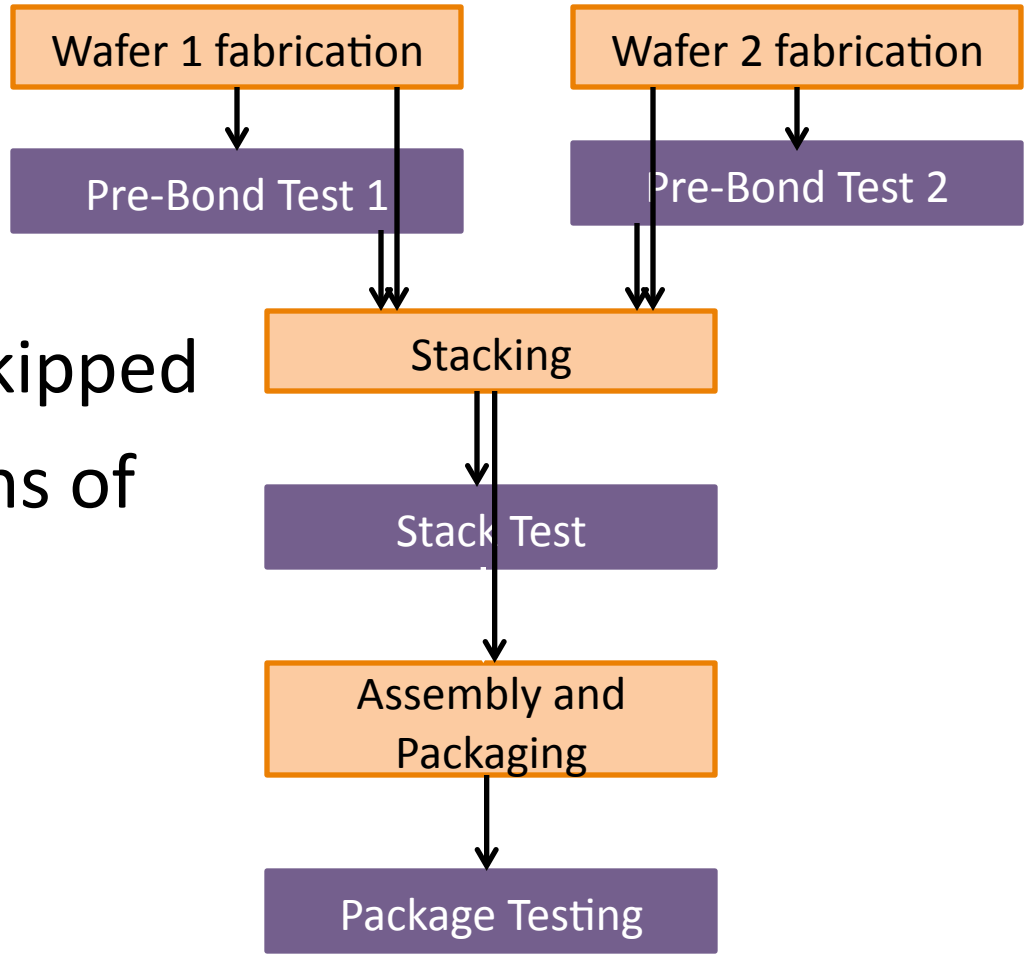
Test Flows

- Pre-bond test 1 skipped



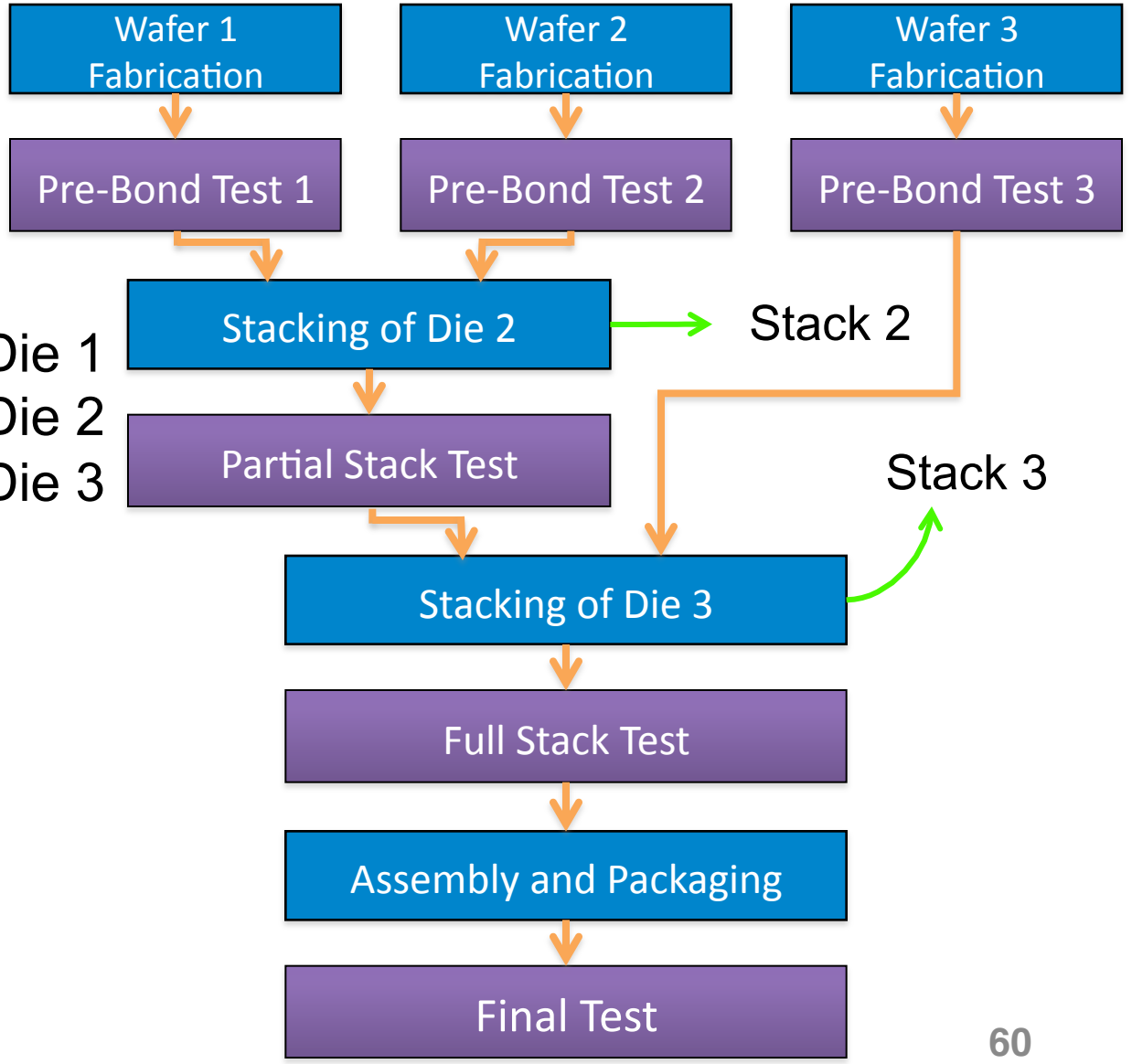
Test Flows

- All test insertions skipped
- 2^4 = 16 combinations of test insertions



Test Flows in a 3-Die Stack

- 3 test insertions for Die 1
- 3 test insertions for Die 2
- 2 test insertions for Die 3
- 8 test insertions
- 256 combinations

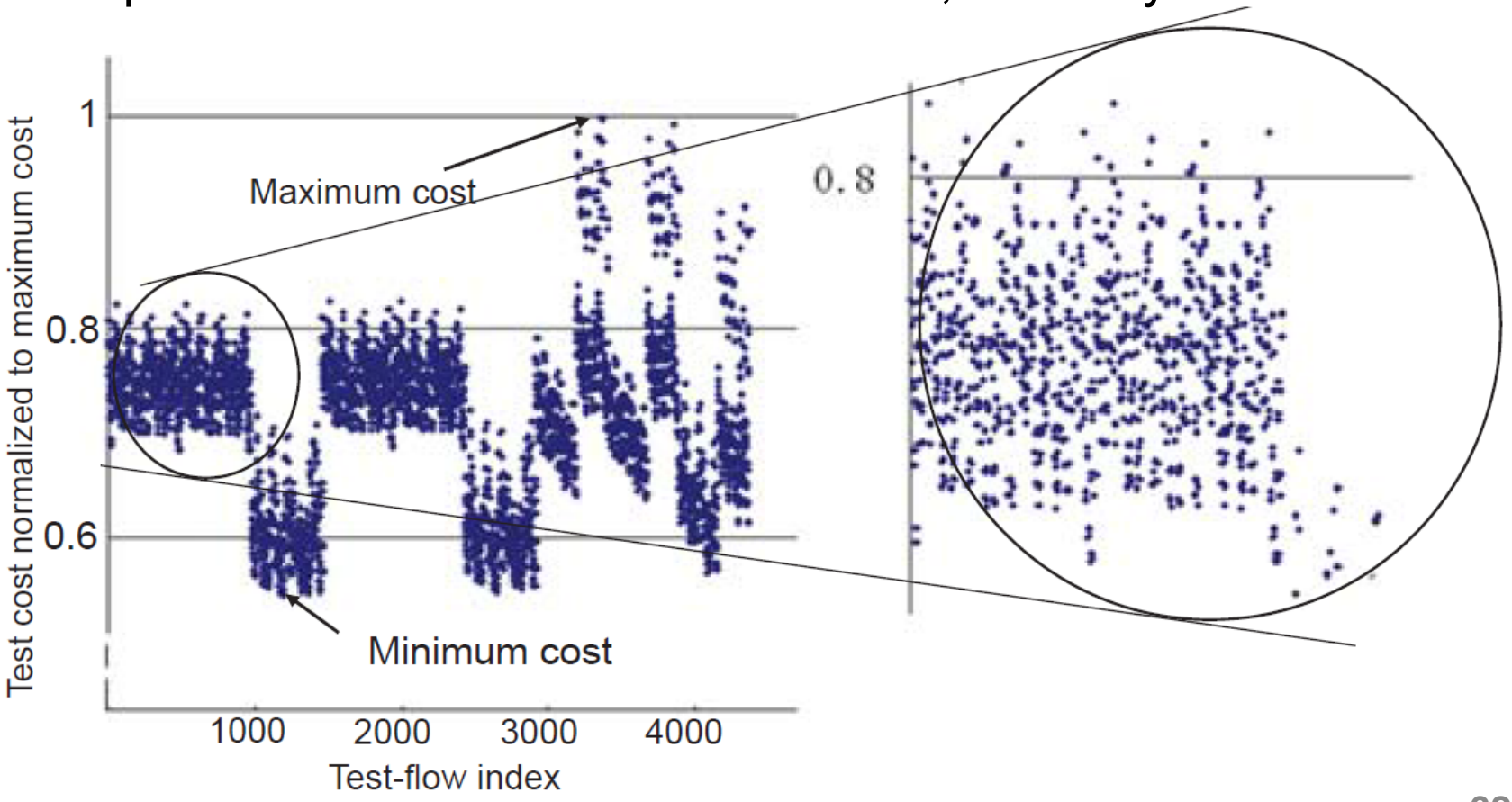


Multiple Types of Tests and Test-Cost Components

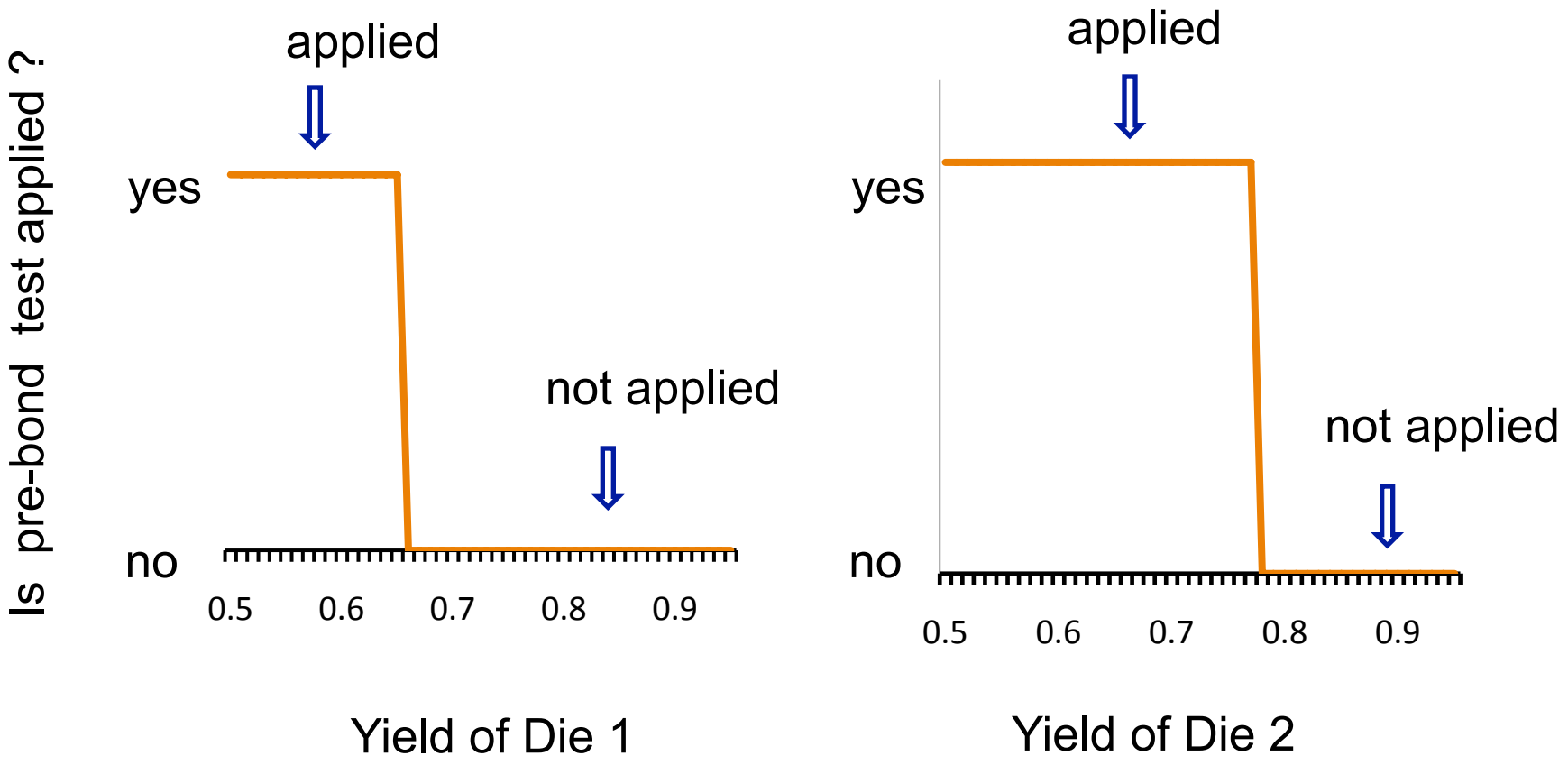
- Stuck-at, Transition, etc.?
- Cost varies on the type and method of test application
  - Cost due to logic implemented on DUT board, load board, etc.
  - Logistic cost associated if the test center is different from the manufacturing center
- Fault coverage?
- Number of possible flows?
- Rigorous mathematical model has been developed

How Many Test Flows?

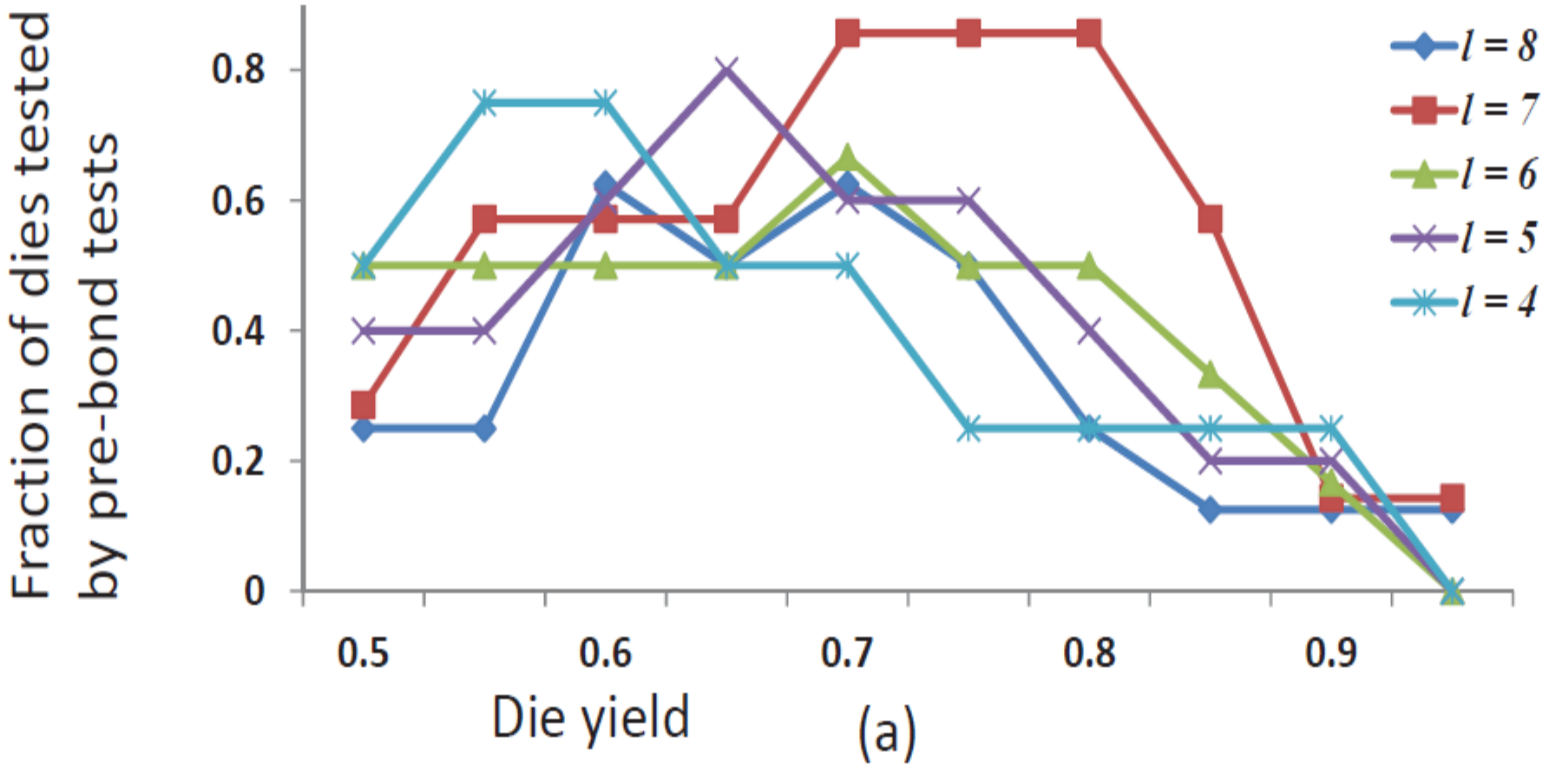
- Exhaustively enumerate all possible candidates
- 2 pre-bond tests for each die to choose from
- 2 post-bond tests for Die 1 and Die 2, and only one for Die3



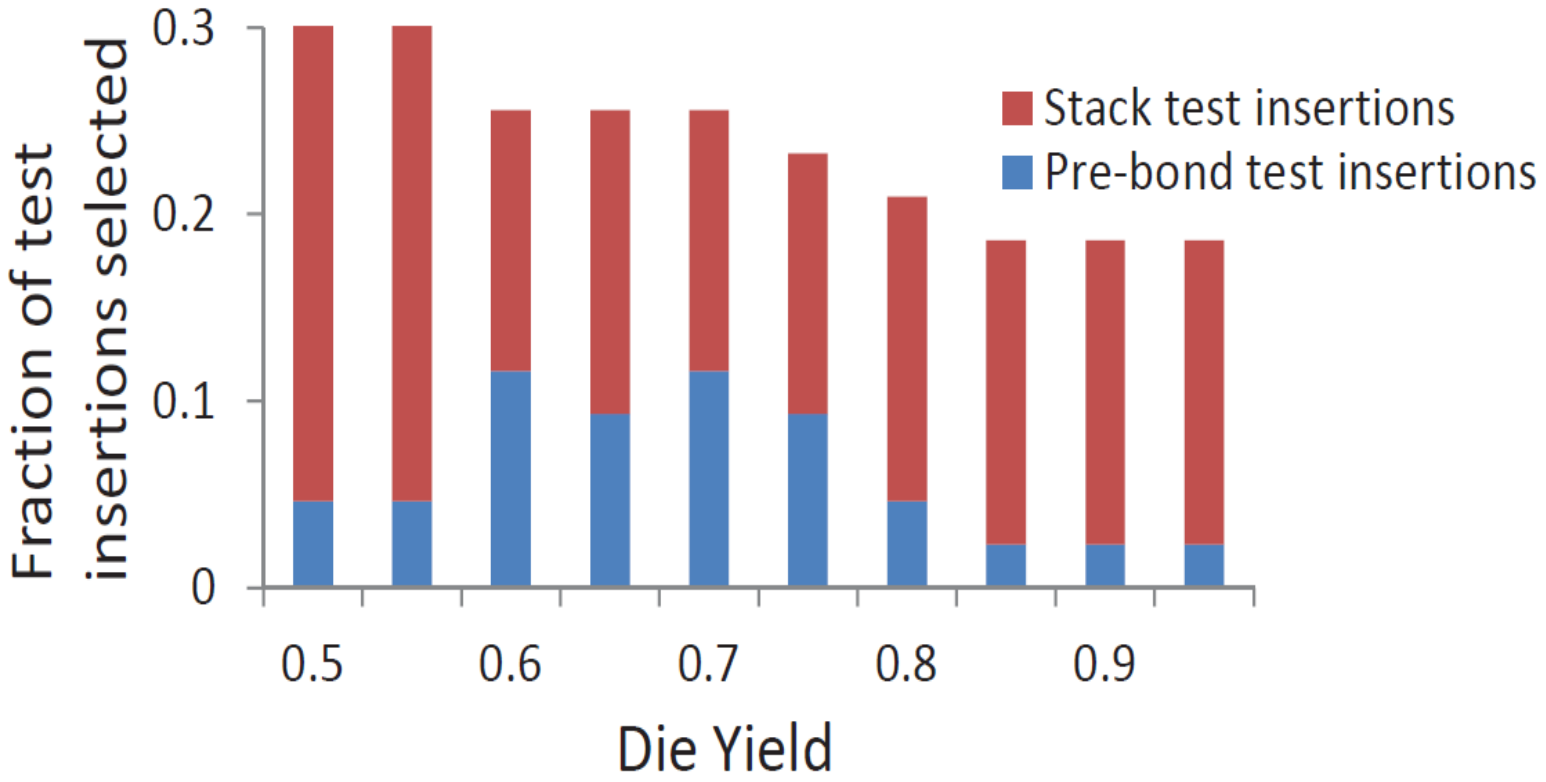
Effect of Die Yield on Selection of Pre-Bond Tests on a 3-Die Stack



Effect of Die Yield on Selection of Pre-Bond Tests

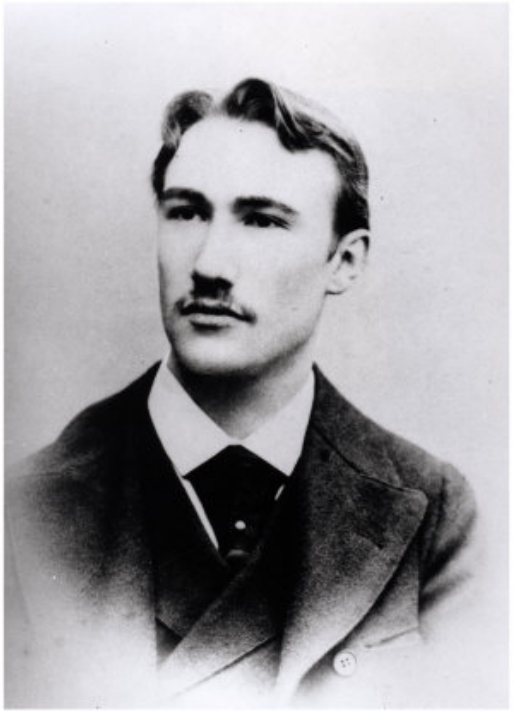


Effect of Die Yield on Overall Test Selection



Conclusions

- 3D fabrication and assembly steps (T
  bonding, thinning, etc.) lead to uniqu
- Known test methods can be utilized (
  p
  -
  - *ore, but since n* *ep*
    over again (An
- C *eeded for of*
  - *SV testing, die*



I shall be telling this with a sigh
Somewhere ages and ages hence:
Two roads diverged in a wood, and I,
I took the one less traveled by,
And that has made all the difference.
(Robert Frost, The Road Not Taken)

One does not discover new lands without consenting to lose sight of the shore for a very long time. (Andre Gide)