Green Chips

Vancouver, November 12-13, 2013

Optimization is the Keyword in NanoCMOs

Ricardo Reis

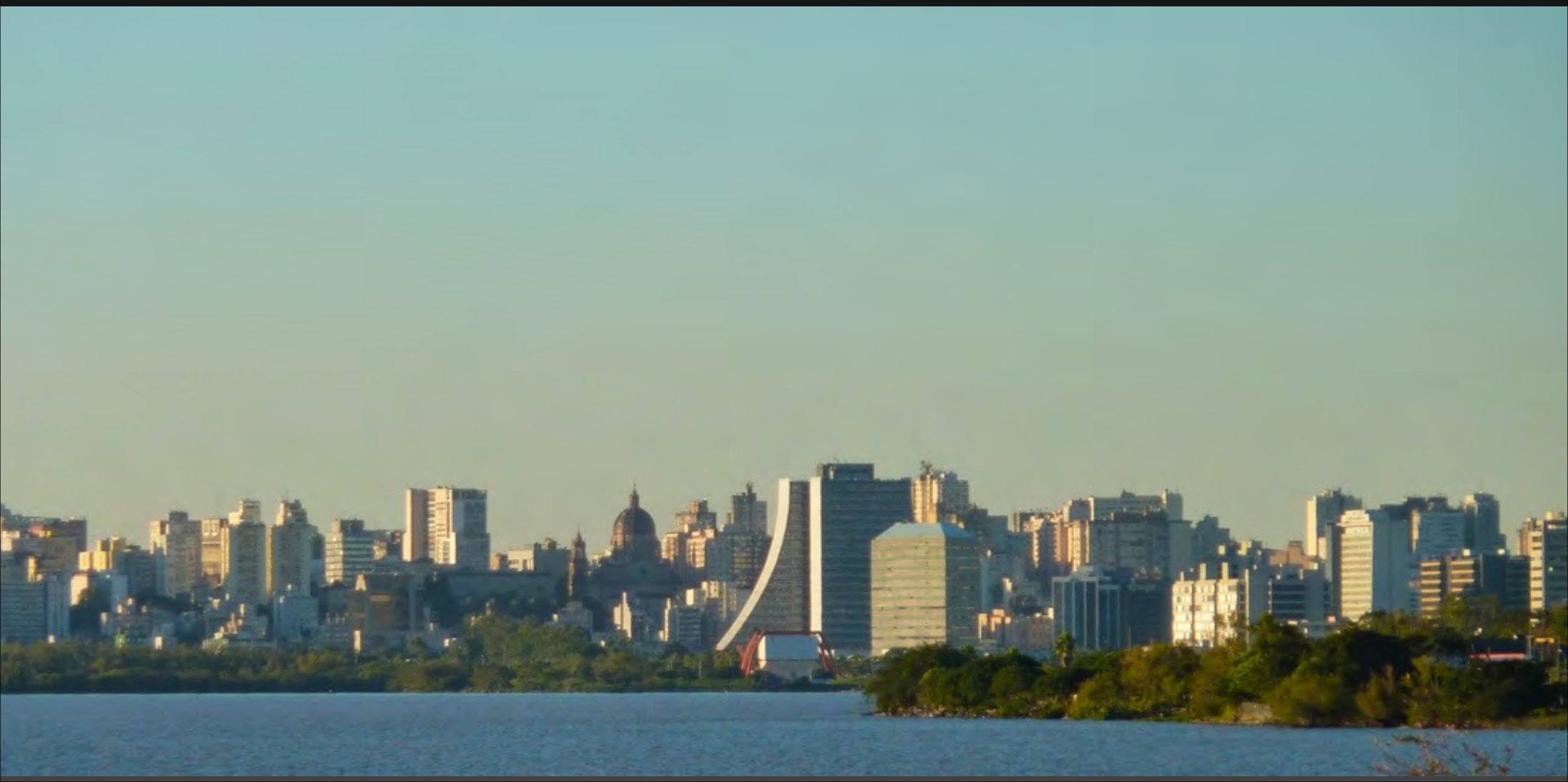
UFRGS

Where
do we come from ...


Porto Alegre

Where do we come from

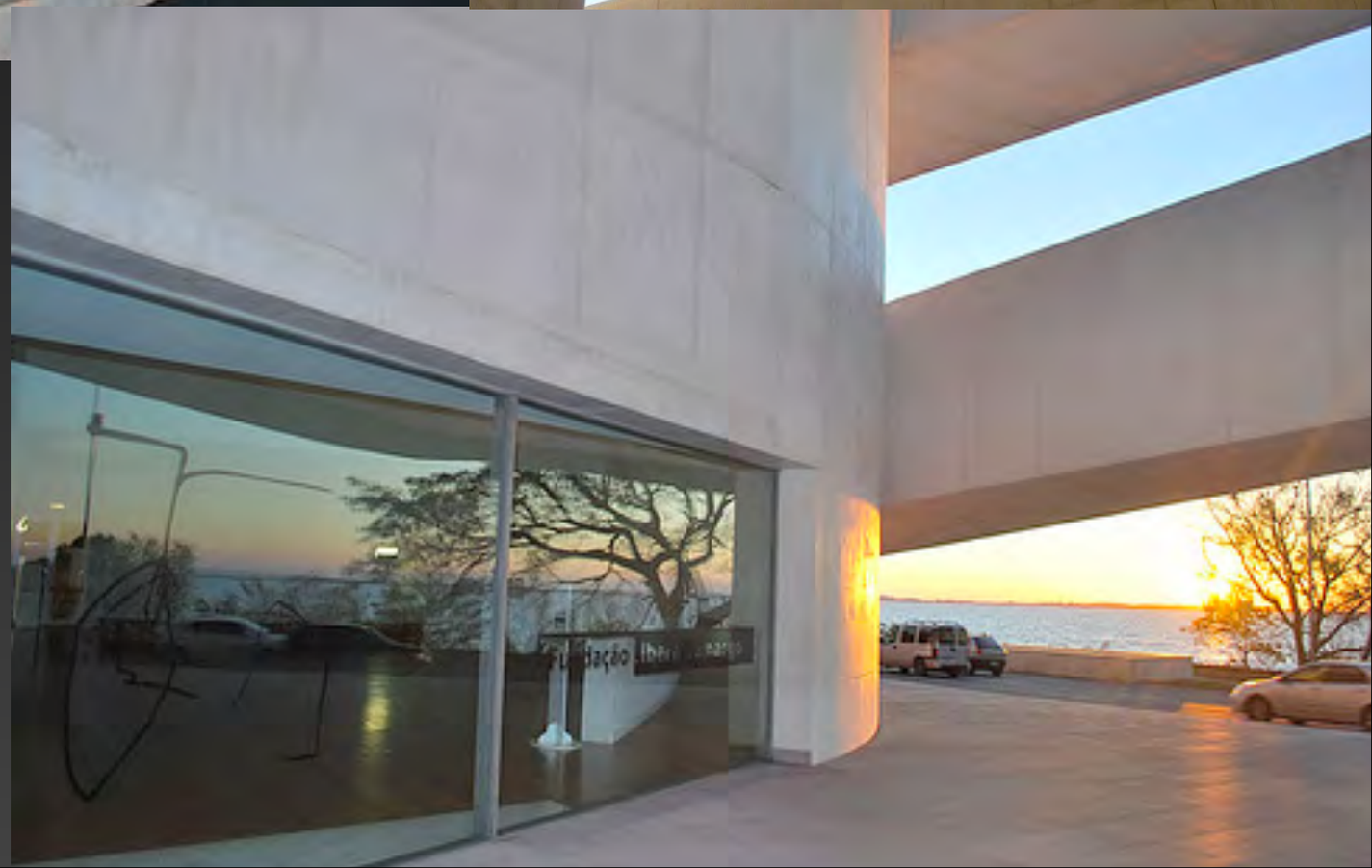
Porto Alegre

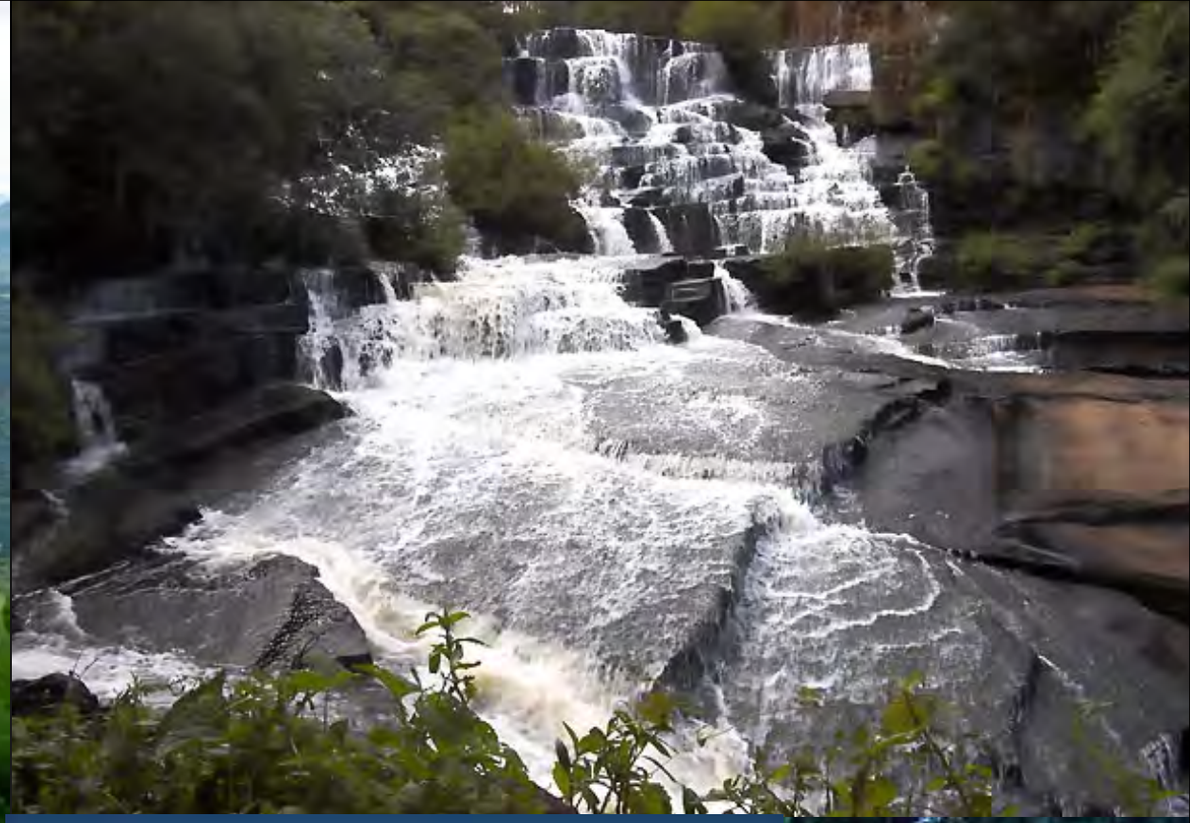


Porto Alegre

Ibere Camargo Museum

Porto Alegre





Instituto de Informática

CEITEC

Design Center - Administrative Building:

Design Center
Process Engineering
Adm. Offices
Teaching Rooms
Auditorium
5.100 m²

Manufacturing Building

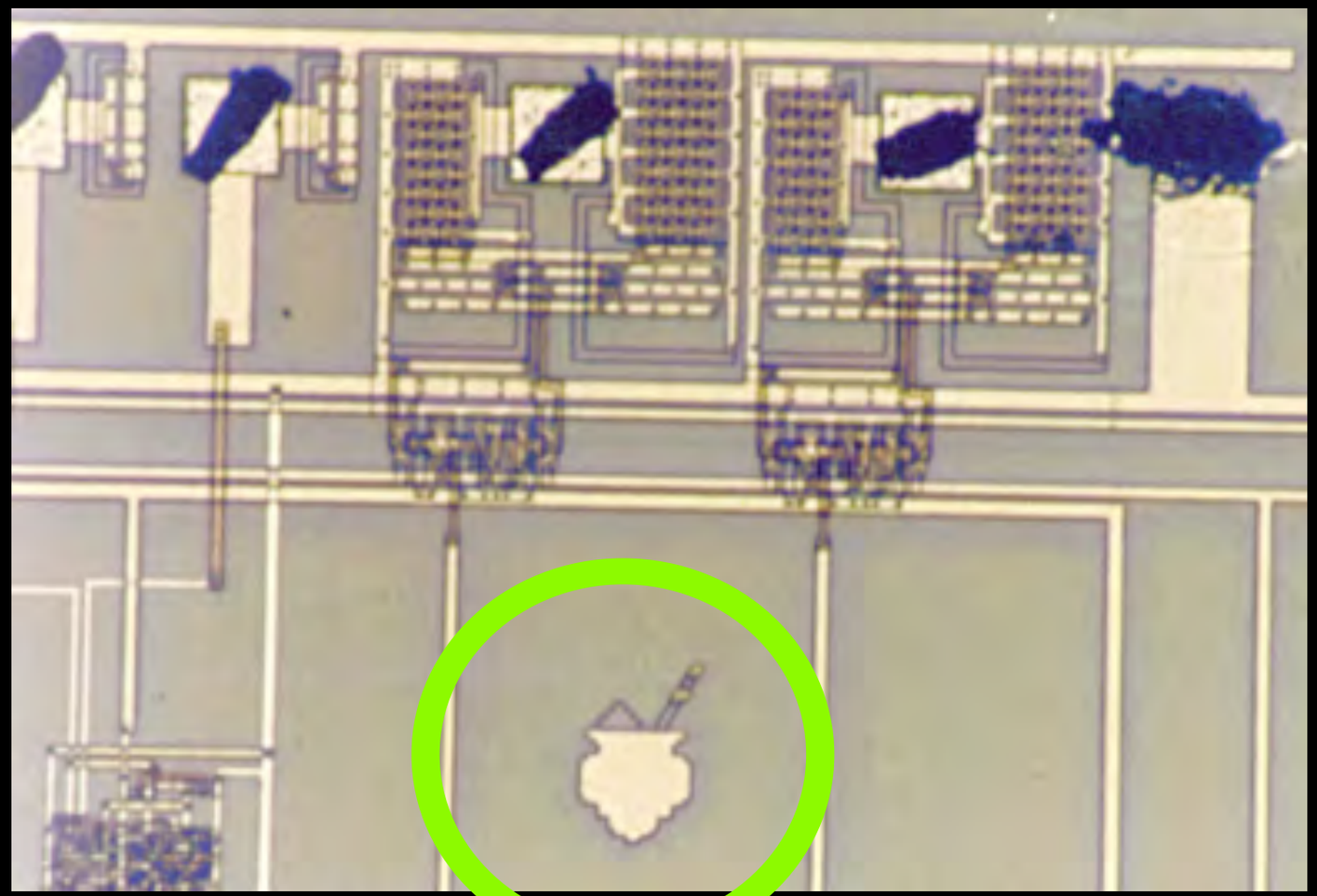
Manufacturing Cleanroom
Research & Development Cleanroom
Facilities and Support
9.600 m²

4.000 wafers/month (200 a 15.000 chips/ wafers)

CEITEC

A bit of History

1984 – Access to MPW prototyping (fabricated at ES2, France)

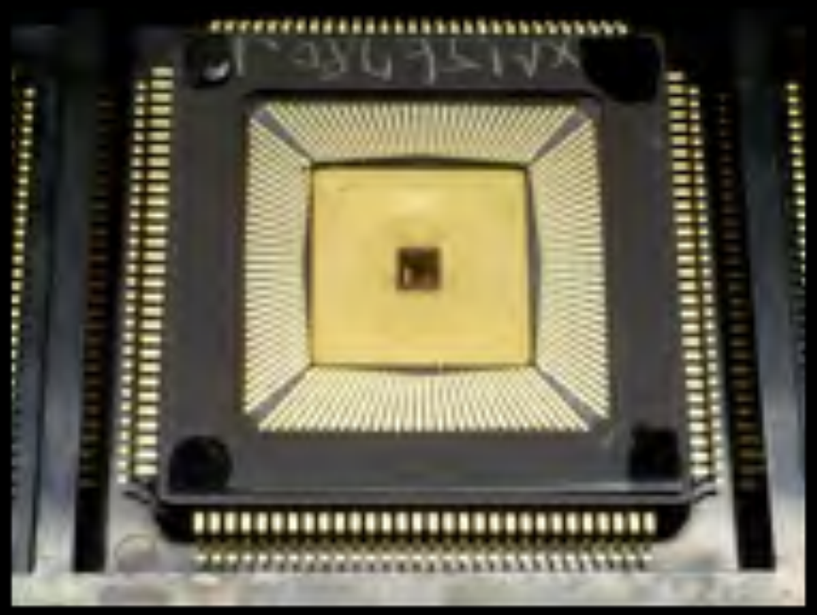


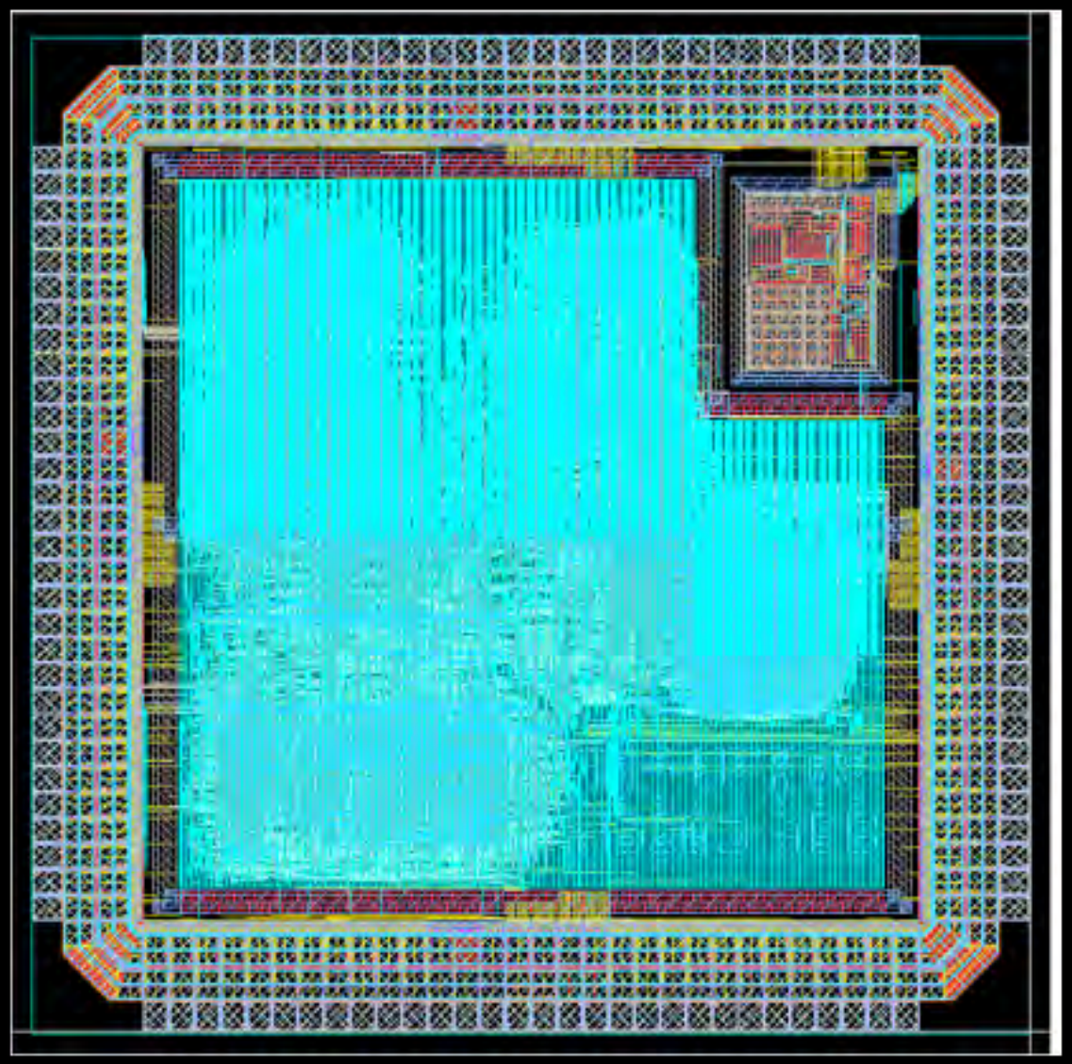
1986 – RISCO 16b/32b completed
First RISC Microprocessor in Brazil (Architecture to Layout)

2012

TMR MIPS Duo Core 32 bits

chip tolerant radiation effects

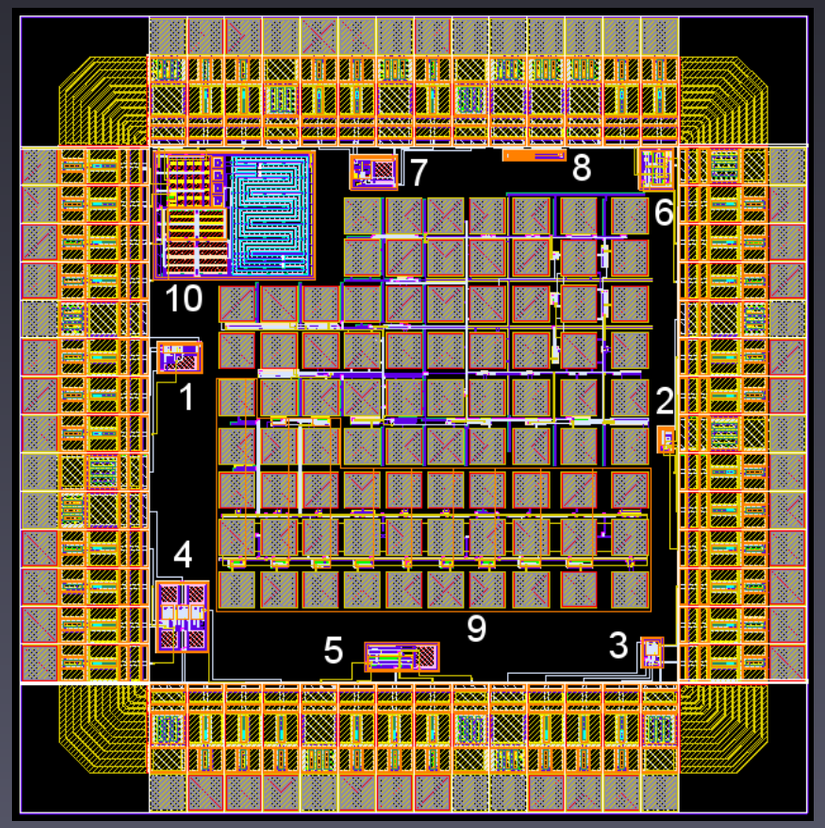


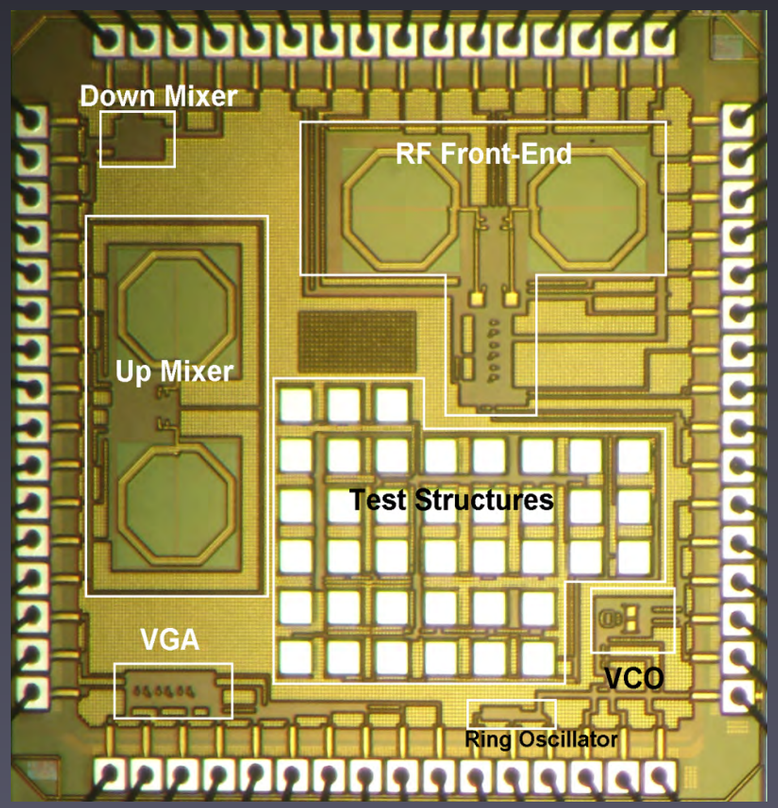


see more at: http://www.nscad.org.br/site/nsc21101

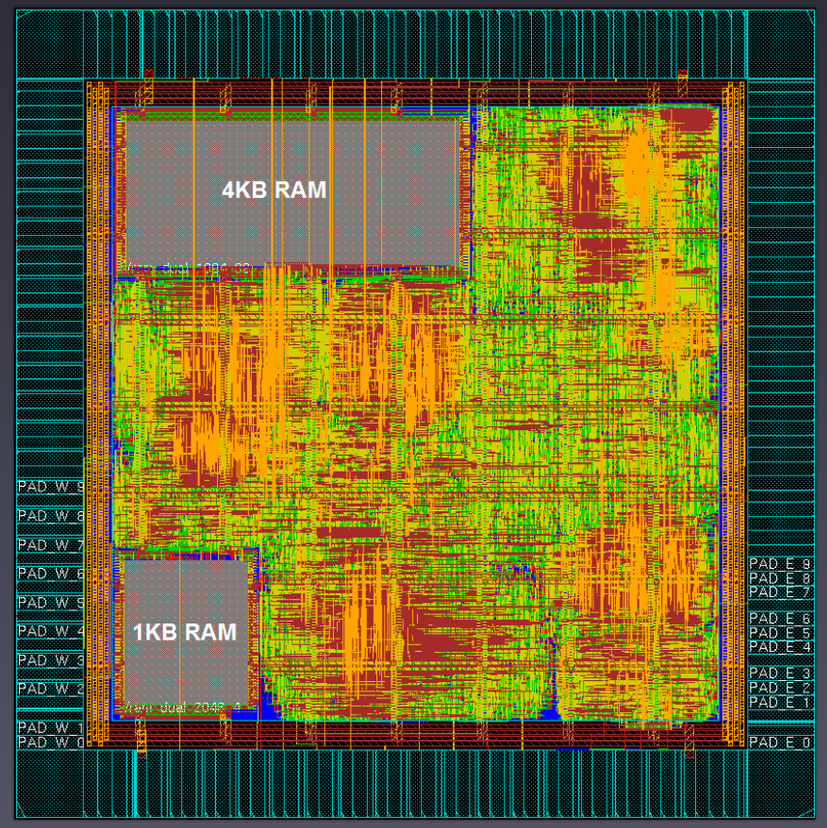
Microelectronics Group Research Topics

- Embedded Systems
- Analog Design
- Digital Design
- Design Methodologies
- VLSI Architectures and Dedicated Architectures
- Digital TV





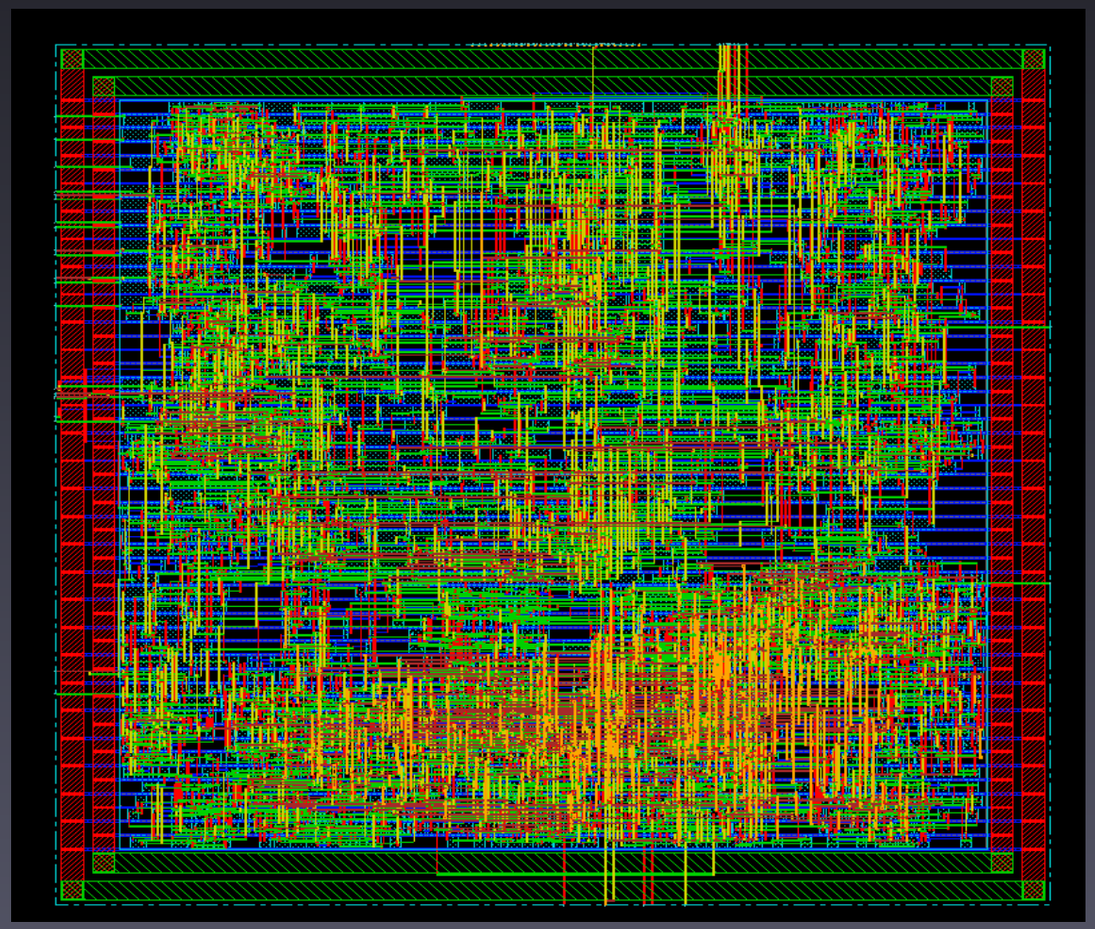
A Multi-Band RF Front End interface



A block of the video decoder

Microelectronics Group Research Topics

- SoC - Systems on a Chip
- NoC - Networks on Chip
- MEMs
- DSP Systems (video, voice, image)
- FPGA Design Methodologies



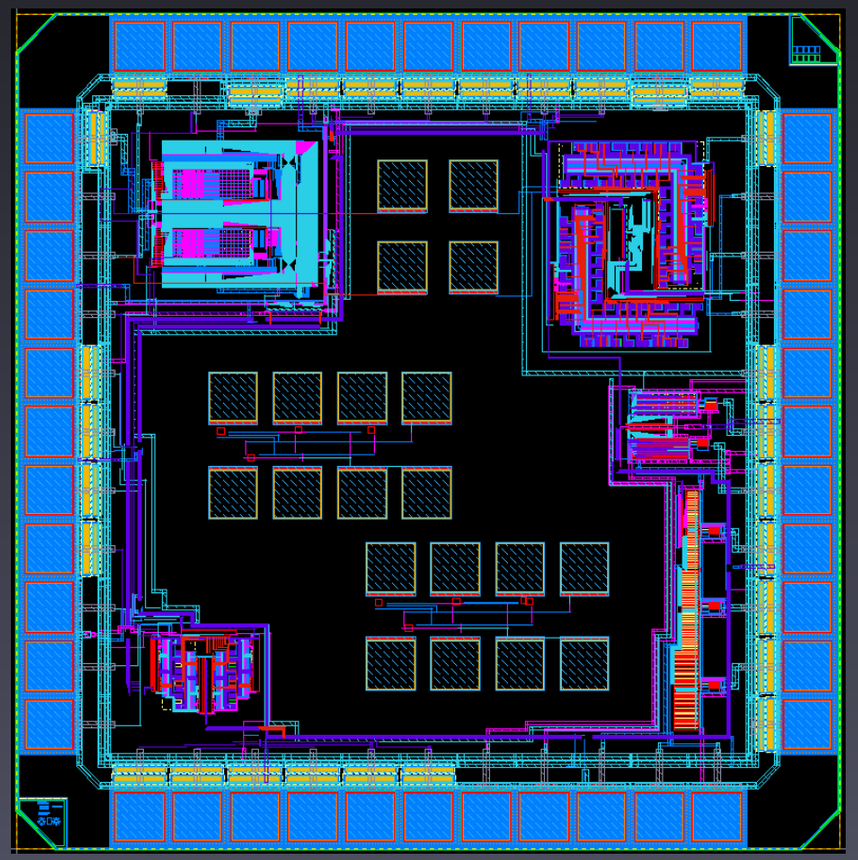
ASIC - CA-VL Coding module
CABAC coder/decoder - Parser

FPGA H.264 Coder prototyping

Microelectronics Group Research Topics

- Fault Tolerant Circuits
- Circuits Tolerant to Radiation Effects
- Variability
- Test
- Mixed Signal

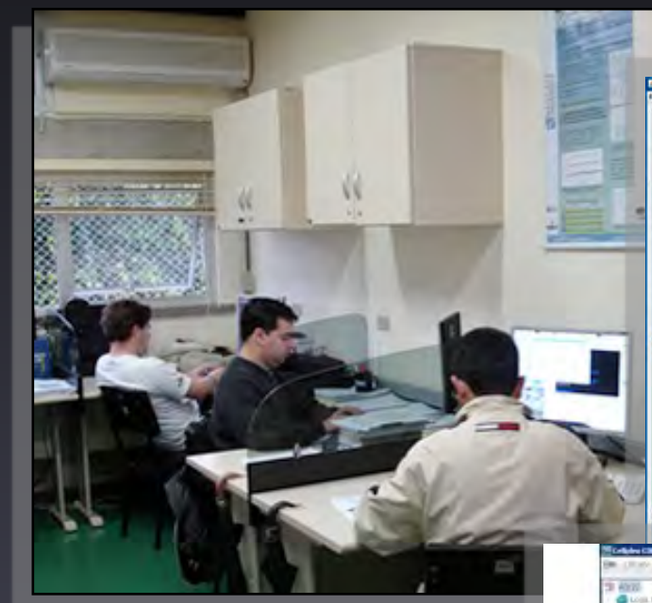
Electrical testing of RFID 915MHz
(CEITEC Design)

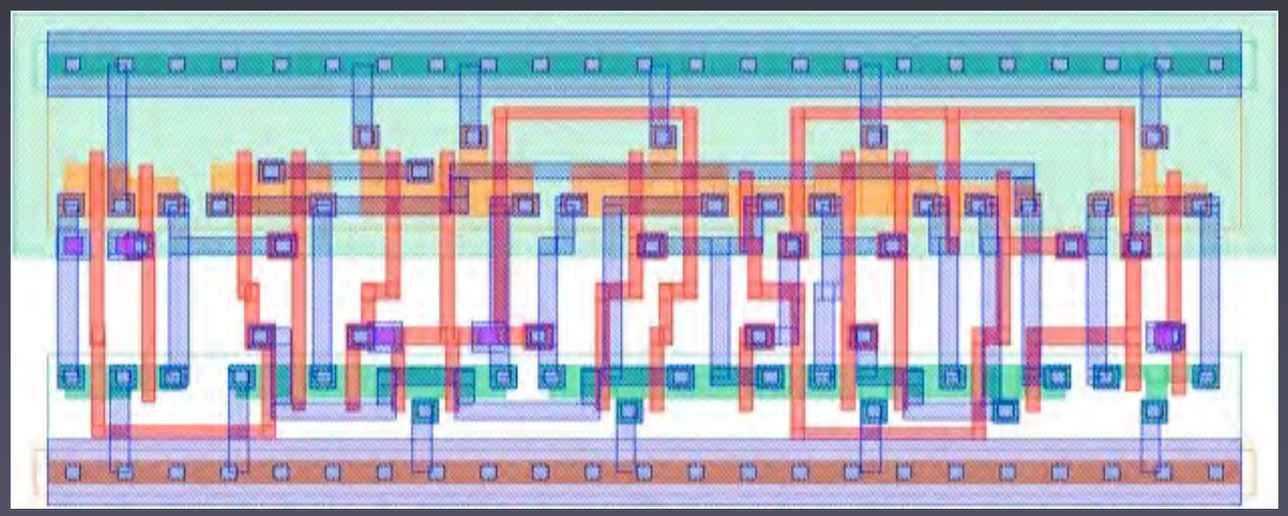


65nm CMOS Variability test structures

Microelectronics Group Research Topics

- Logic Synthesis
- Physical Design
- Design of Transistor Networks
- EDA Tools





Designed Automatically with ASTRAN

Optimization is the Keyword in NanoCMOs

by Ricardo Reis

OUTLINE

1. Introduction
2. Standard Cell
3. Power Reduction by using CMOS Complex Gates
4. Automatic Layout Synthesis
5. Experimental Results
6. Conclusions

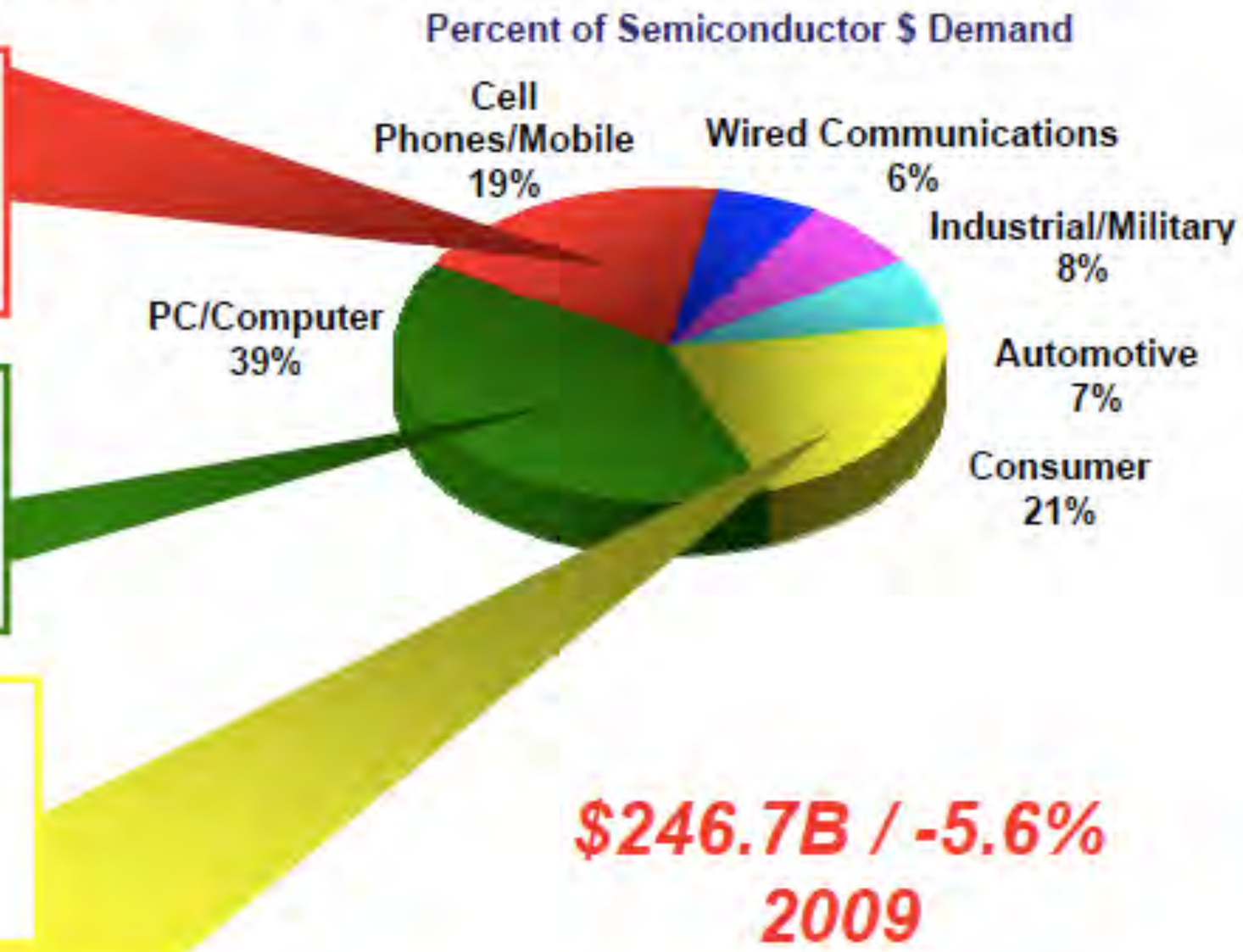
Semiconductor Demand Drivers: 2009 Outlook

2009
Cell Phone Shipments
-6.4% *(units)*

2009
PC Shipments
-5% *(Units)*

2009
PMP/MP3
+8% *(Units)*

2009
Digital Still Camera
+7% *(Units)*



$246.7B / -5.6%
2009

Sources: SIA Fall 2008 Forecast/iSuppli/ Deutsche Bank Securities Inc.
Note: Military is <1% and is included in Industrial.

SIA SEMICONDUCTOR INDUSTRY ASSOCIATION

45

28

22

14

nm

2 Main Problems in NanoCMOS

VARIABILITY

POWER (mainly Static Power)

VARIABILITY

VARIABILITY

VARIABILITY VARIABILITY

VARIABILITY VARIABILITY

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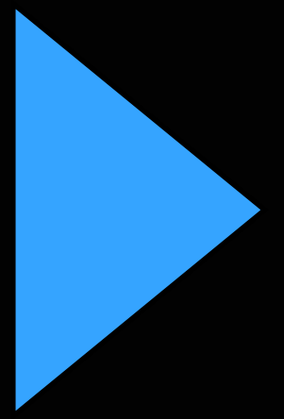
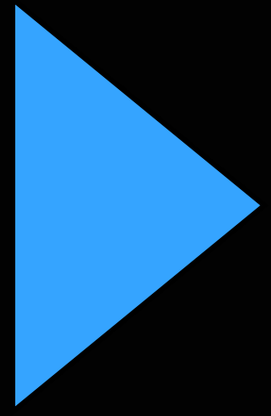
VARIABILITY

VARIABILITY 60
VARIABILITY 56



4 points

VARIABILITY 12
VARIABILITY 8



4 points

Sources/Types of Variability

Fabrication Technology

Environment

Aging


Why Optimization is a Keyword in NanoCMOS?

More em More

Embedded Systems

that requires Low Power

Design Levels of Abstraction

Estimation Tools

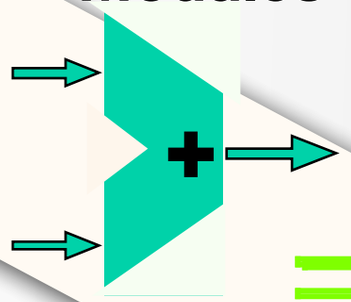
Power

Performance

Number of Transistors

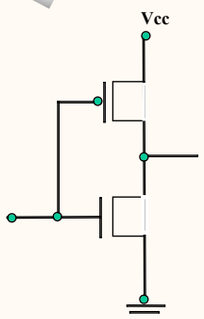
System

Modules

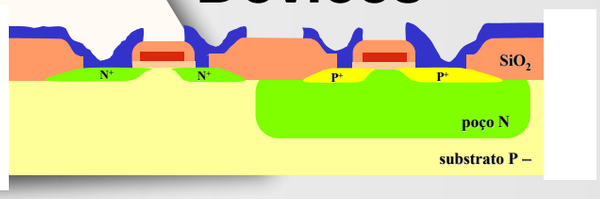


Logic Gates

Circuit



Devices



UFRGS

GME

Ricardo Reis

Power Reduction at Physical Level

Gate Sizing

Reduction on the amount of transistors

ISPD - International Symposium on Physical Design
Discrete Gate Sizing Contest 2012 and 2013

organized by Intel

Tiago Reimann, Guilherme Flach, Gracieli Posser
Jozeanne Belomo, Marcelo Johann, Ricardo Reis

UFRGS

A grain of rice has the price of more than a100 thousand transistors

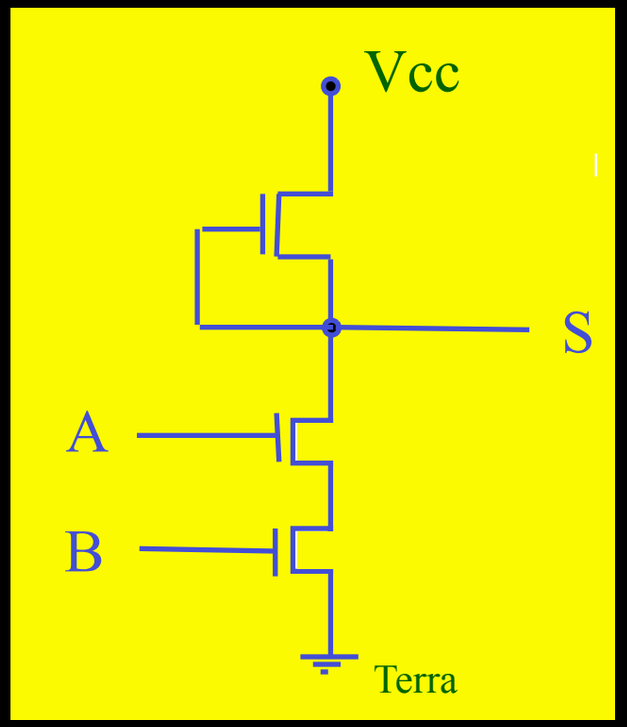
Source: The Economist, September 6, 2010

A transistor is cheap

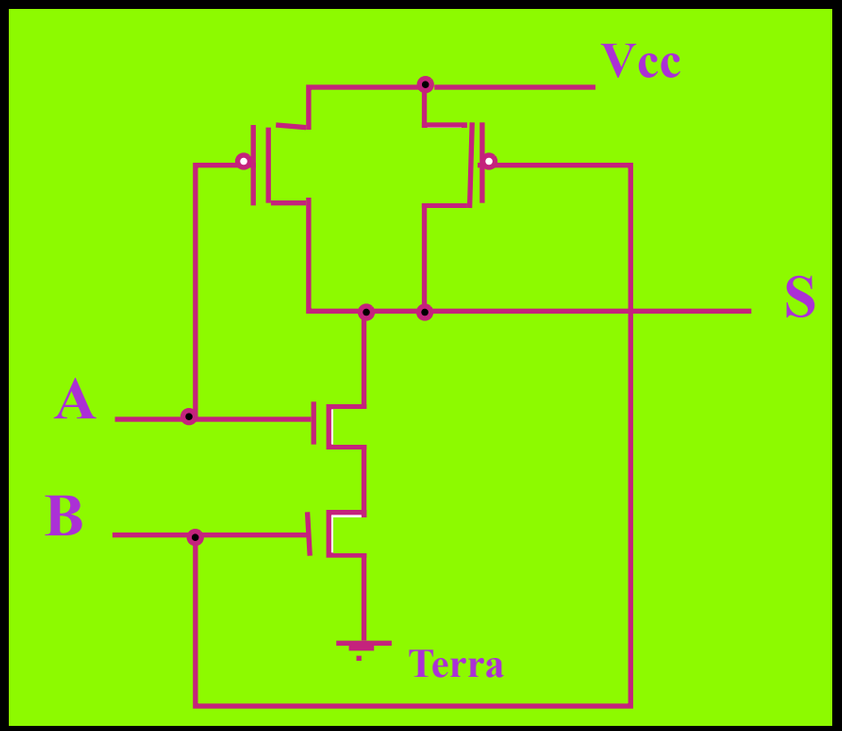
BUT

Energy is expensive

Power Consumption drives MOS evolution



NMOS



CMOS

Challenge:

Power Optimization must be done in all levels of abstraction

Power Estimation Tools

for each level of abstraction

Power Reduction

Ileakage is become more and more important in nanocircuits

It is function of the number of transistors

LESS TRANSISTORS MEANS LESS LEAKAGE POWER

Standard Cell Approach

Cell characterization

Cell performance predictability

But nowadays cell predictability is not anymore sufficient to have circuit predictability

Connections becomes a central problem !

Standard Cell Approach

Logic Options Limited to Cells Available in the Library

No optimal logic minimization

Cells oversized

Area

Standard Cell Approach

Far from Minimization on:

- Area
- Number of Transistors
- Wirelenght
- Delay
- Power

History

Logic Design Evolution

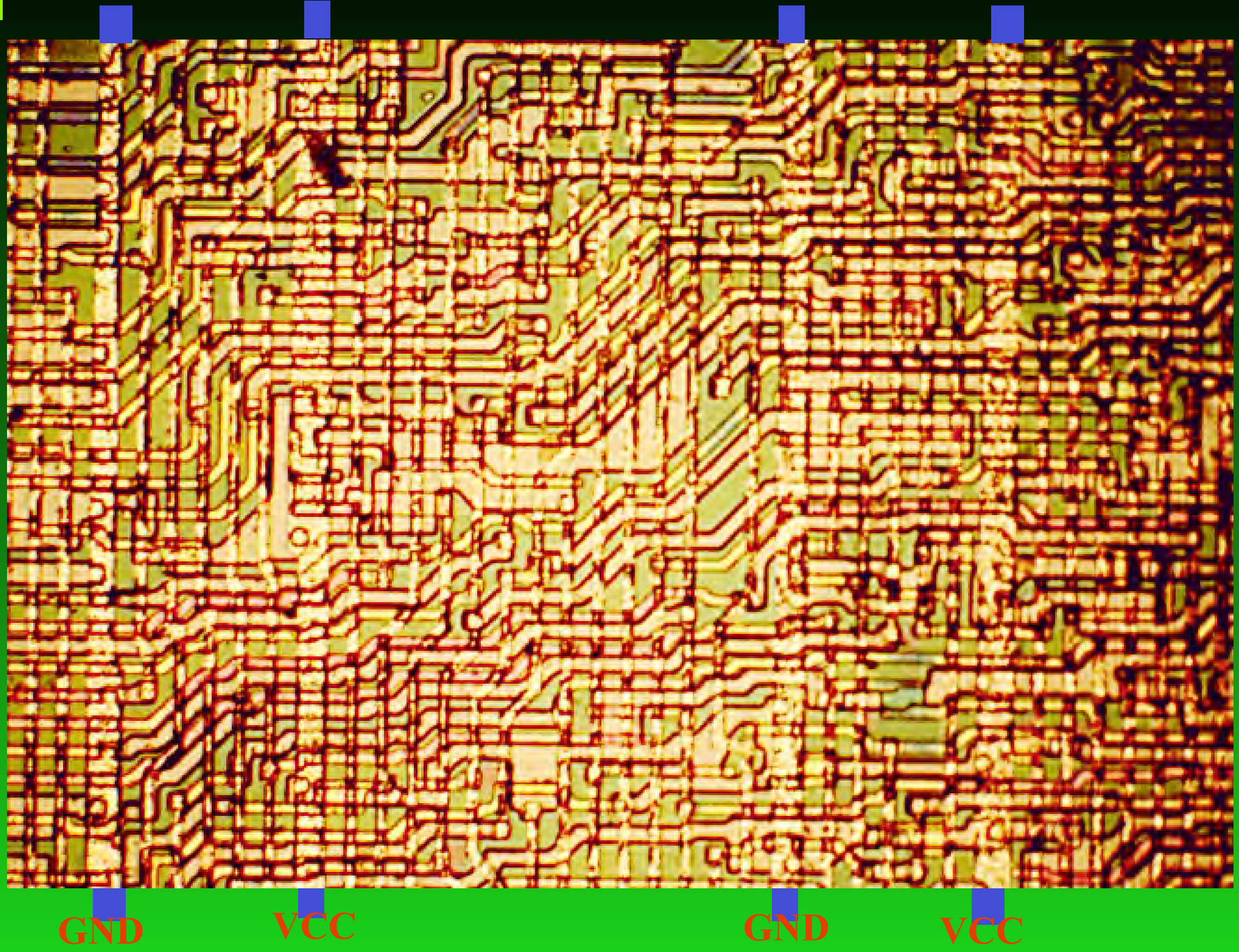
Years 70 : microprocessors “hand made”
computer used just as graphical input

End Years 70: Random Logic → ROMs, PLAs
Z8000 → **M68000**

Years 90: ROMs, PLAs → Standard Cell
486, Pentium

Next Step: Standard Cell → Random Logic
Automatic Layout of Cells-on-the-fly

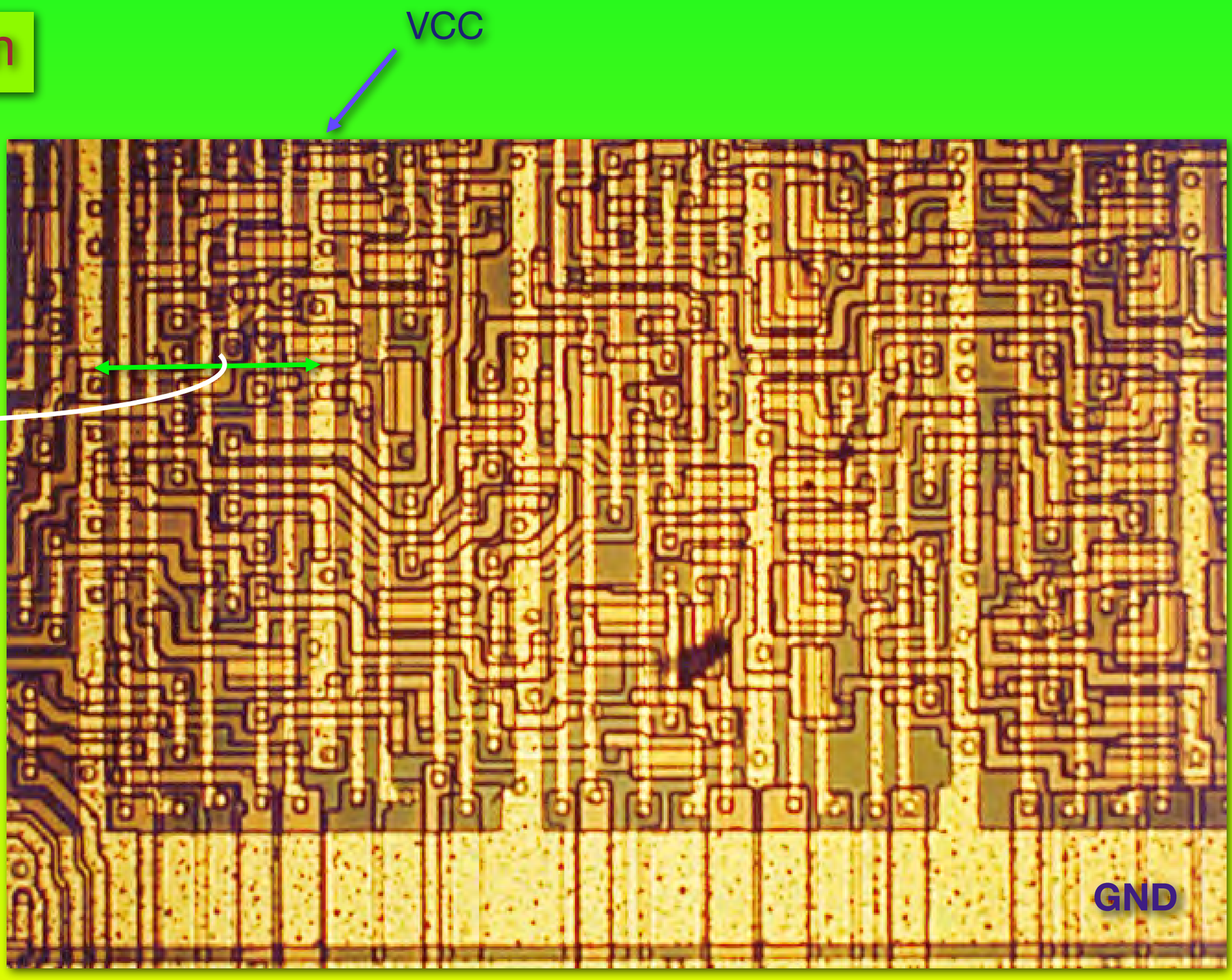
Full Custom



Zilog Z8000

detail of the control part using random logic

Full Custom



Detail of the control part of TMS7000 implemented with random logic

Break the Wall

Change of Paradigm

Cell Generation on-the-fly

physical design as the design of a network of transistors

Standard Cell Approach

X

Cell On-the-fly Approach

Transistor Level Design Automation

Connections becomes
a central problem !

Challenge:
how to reduce wirelength?

Challenge:

how to reduce wirelength?

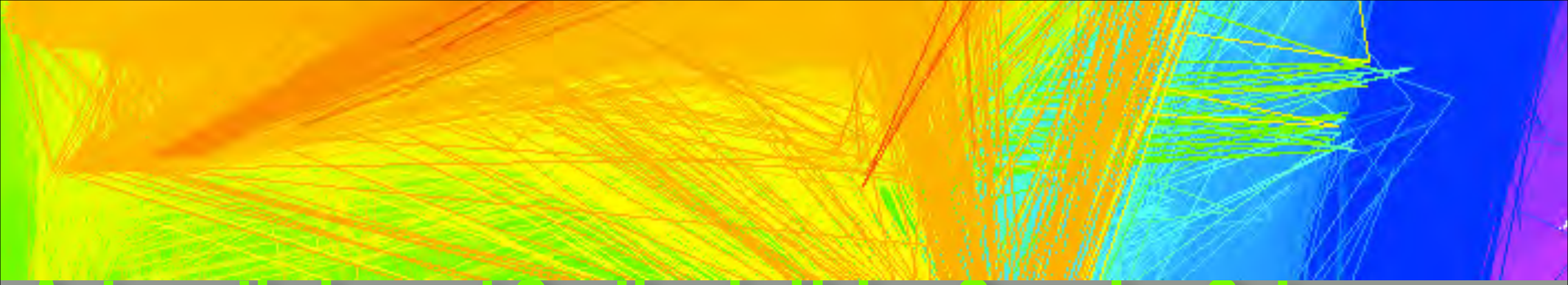
- area reduction
- use of complex gates (SCCG)
- improvement of routing and placement algorithms

Using Static CMOS Complex Gates (SCCG)

with cell generation on-the-fly

It is possible do to an extreme logic minimization

Freedom to Logic Designers !!!!



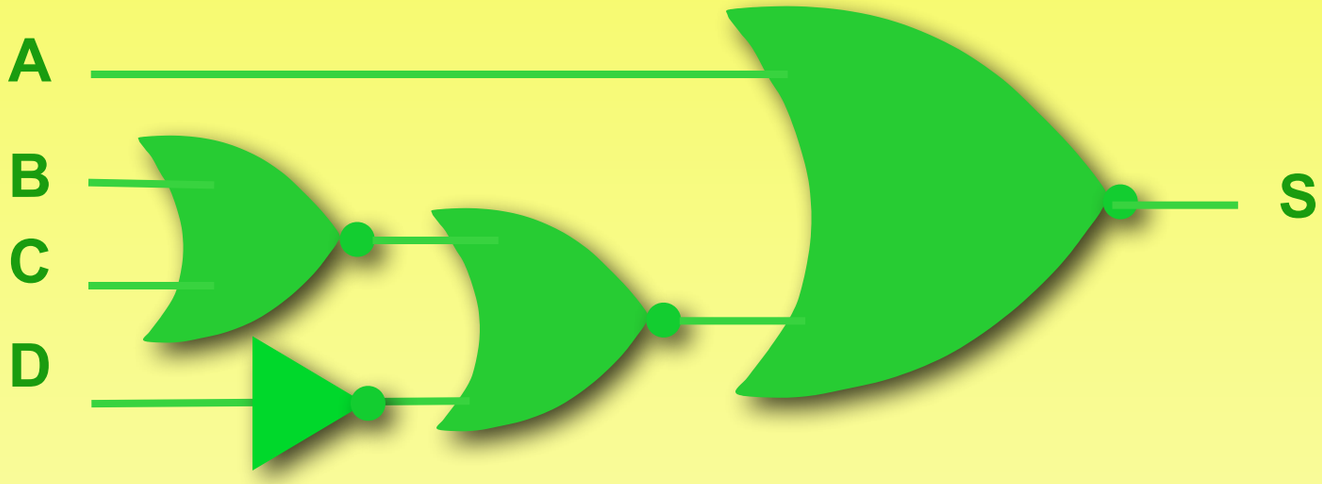
Automatic Layout Synthesis Using Complex Gates (SCCG)

NUMBER OF STACKED PMOS TRANSISTORS

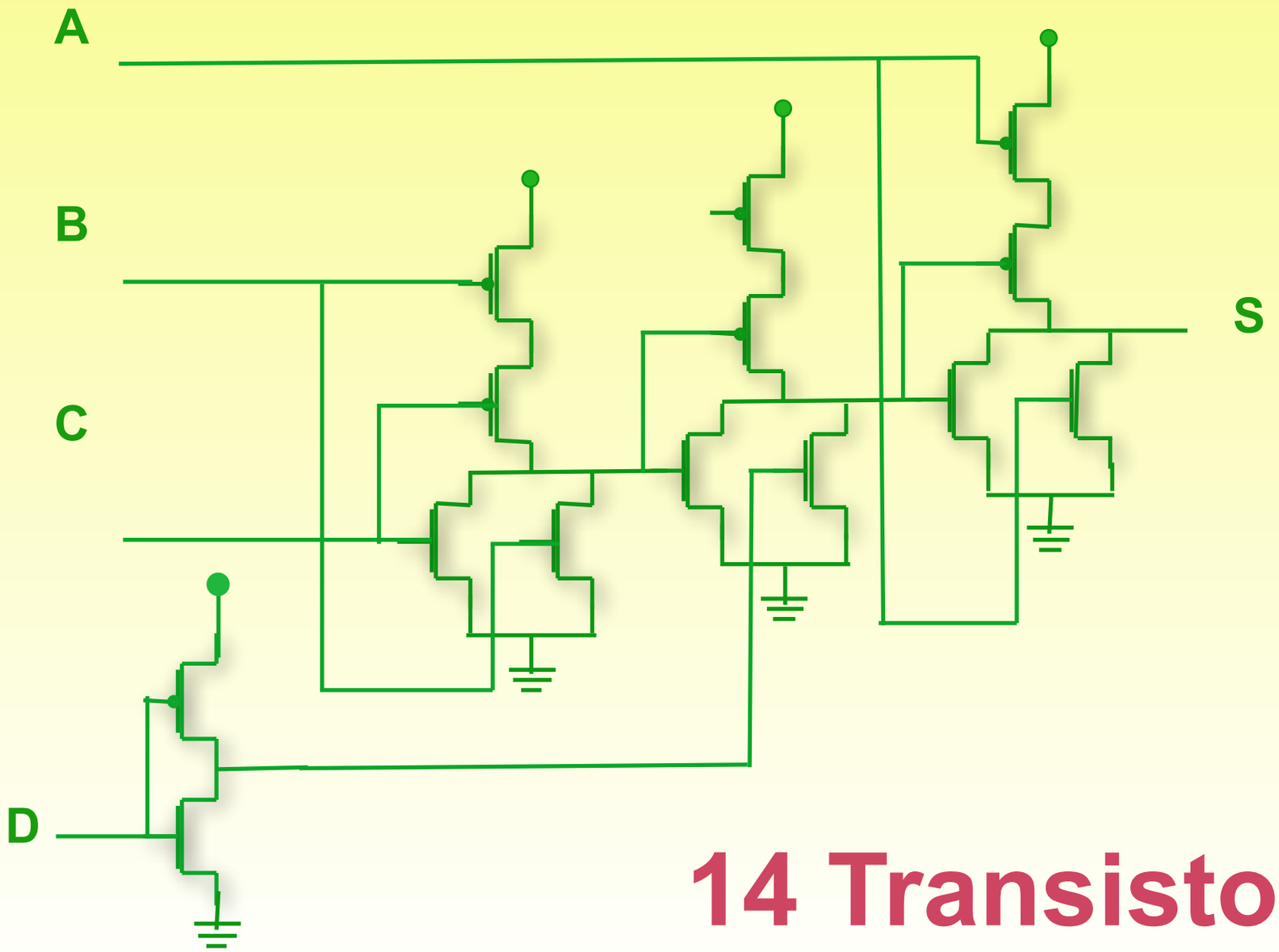
NUMBER OF STACKED NMOS TRANSISTORS	1	2	3	4	5
1	1	2	3	4	5
2	2	7	18	42	90
3	3	18	87	396	1677
4	4	42	396	3503	28435
5	5	90	1677	28435	125803

E. Detjens et al., Technology Mapping in MIS, ICCAD 1987

Example



$$S = A + ((\overline{B + C)} + D)$$

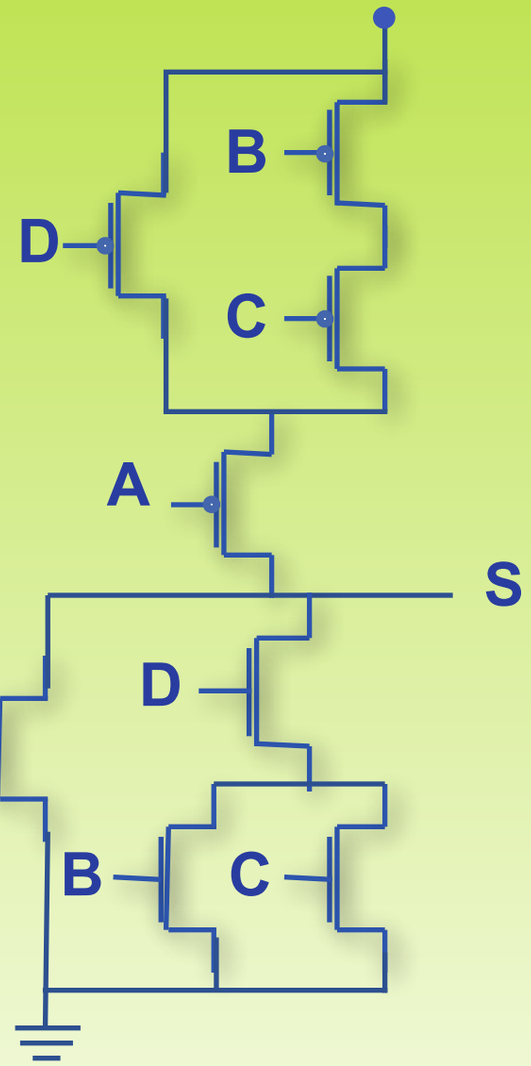


14 Transistors

Use of SCCG

$$S = \overline{A + ((\overline{B + C}) + D)}$$

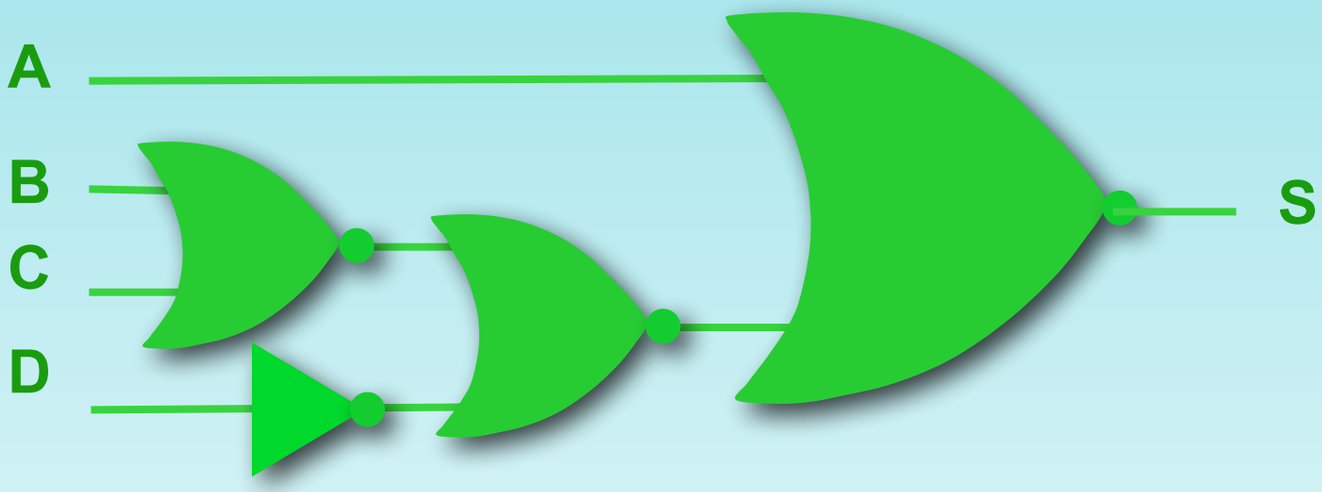
$$S = \overline{A + ((B + C).D)}$$



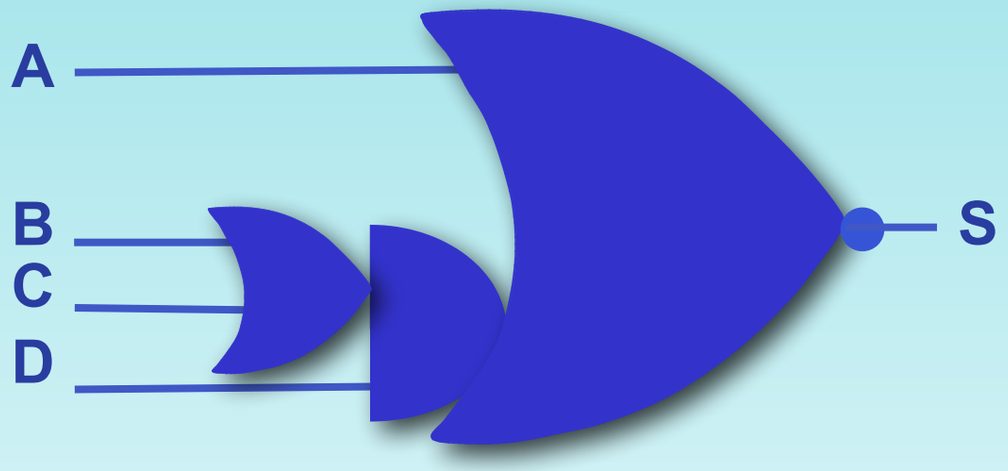
8 Transistors

Use of SCCG

$$S = \overline{A + ((\overline{B + C}) + D)} \quad \Rightarrow \quad S = \overline{A + ((B + C).D)}$$



14 Transistors



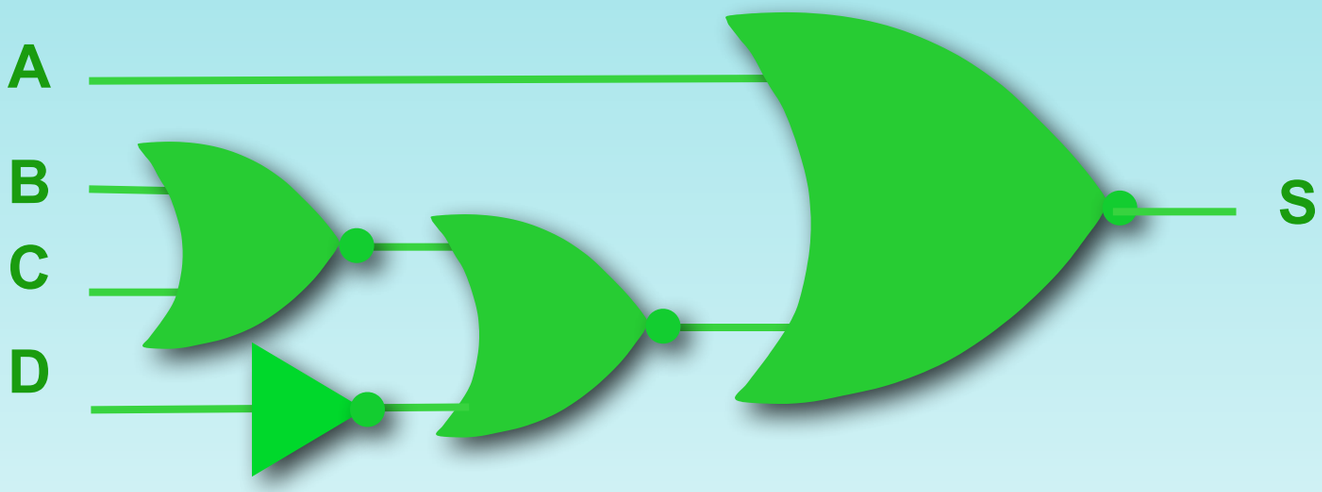
8 Transistors

LESS TRANSISTORS MEANS LESS LEAKAGE POWER

Use of SCCG

$$S = A + ((\overline{B + C}) + D)$$

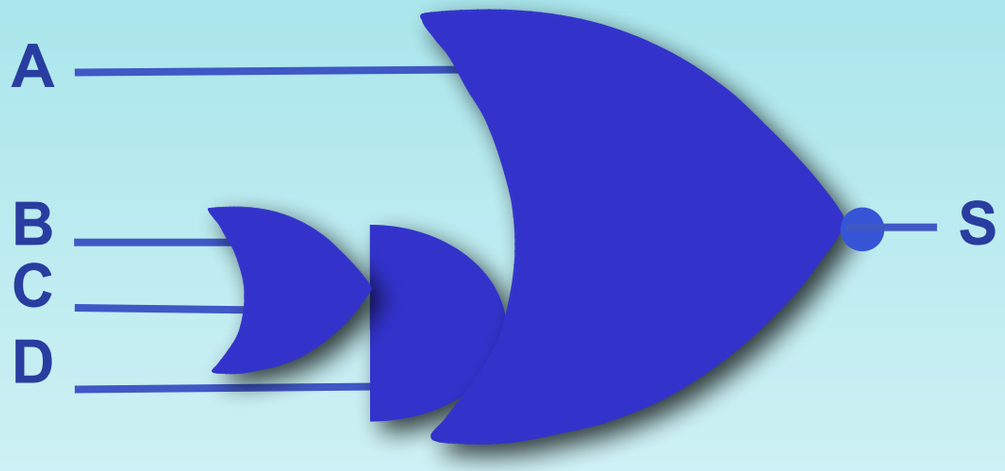
$$S = \overline{A + ((B + C).D)}$$



14 Transistors

+

3 internal connections



8 Transistors

LESS TRANSISTORS ALSO MEANS

LESS

CONNECTIONS

ALSO LESS Logic Cells

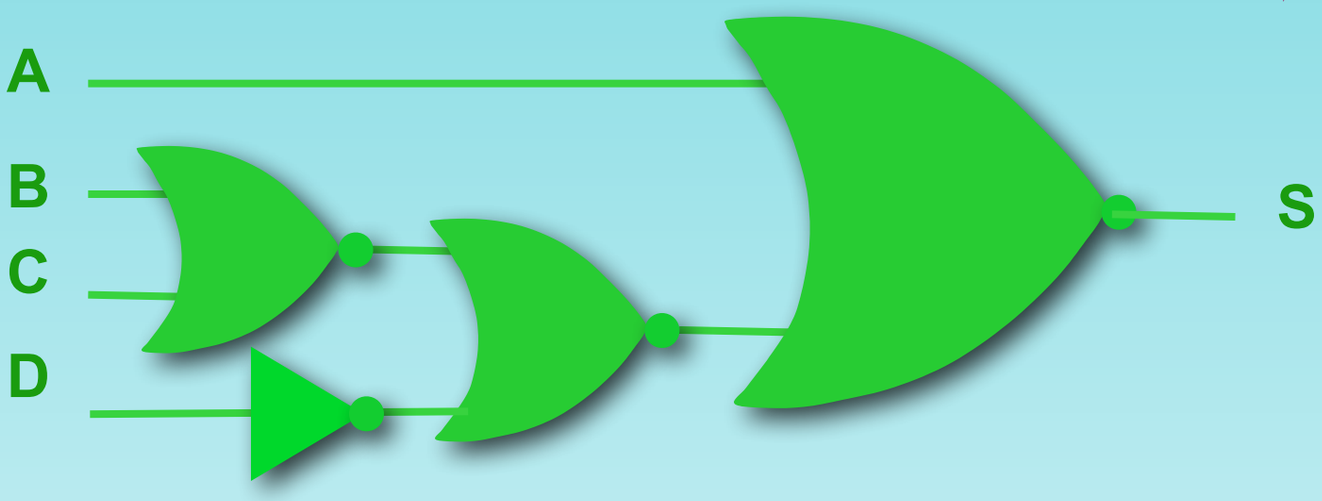
MEANS

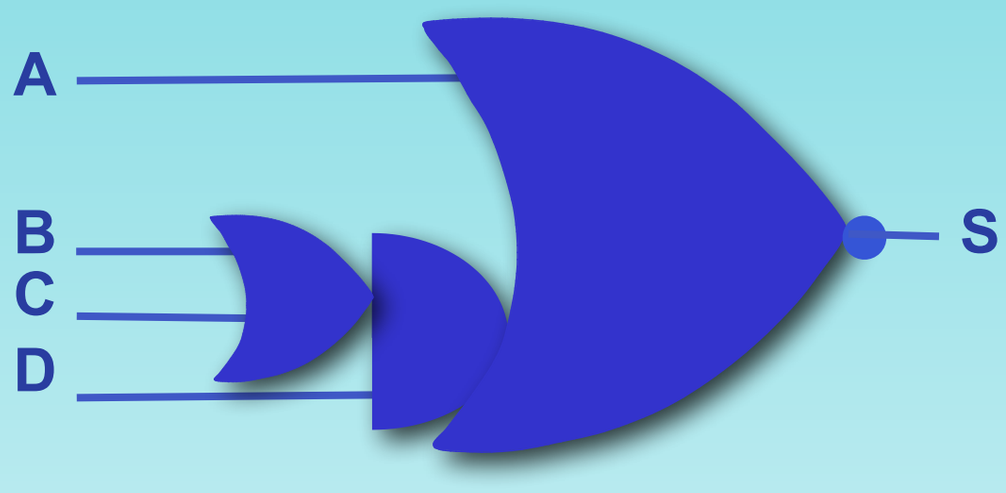
LESS

CONNECTIONS

Use of SCCG

$$S = \overline{A + ((\overline{B + C}) + D)} \quad \Rightarrow \quad S = \overline{A + ((B + C).D)}$$





14 Transistors **8 Transistors**

3 connections less

means also less VIAS

LESS CONNECTIONS

ALSO MEANS

MORE SPACE

BETWEEN CONNECTIONS

Reliability

Increases

To Increase

Reliability

It is needed to reduce

CONNECTION

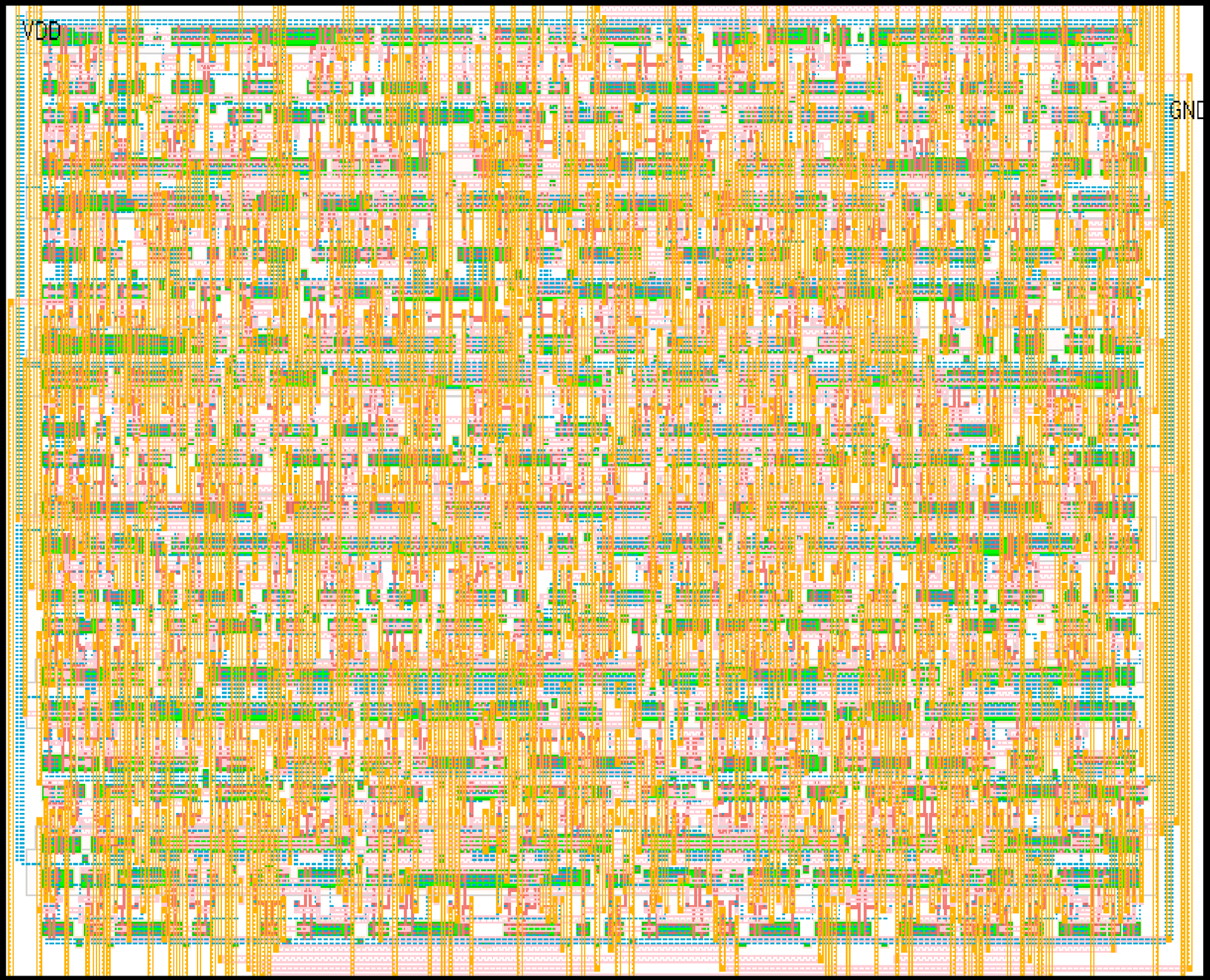
congestions

Layout Strategies

- transistor topologies
- management of routing in all layers
- VCC and Ground distribution
- clock distribution
- contacts and vias management
- body ties management
- transistor sizing and folding

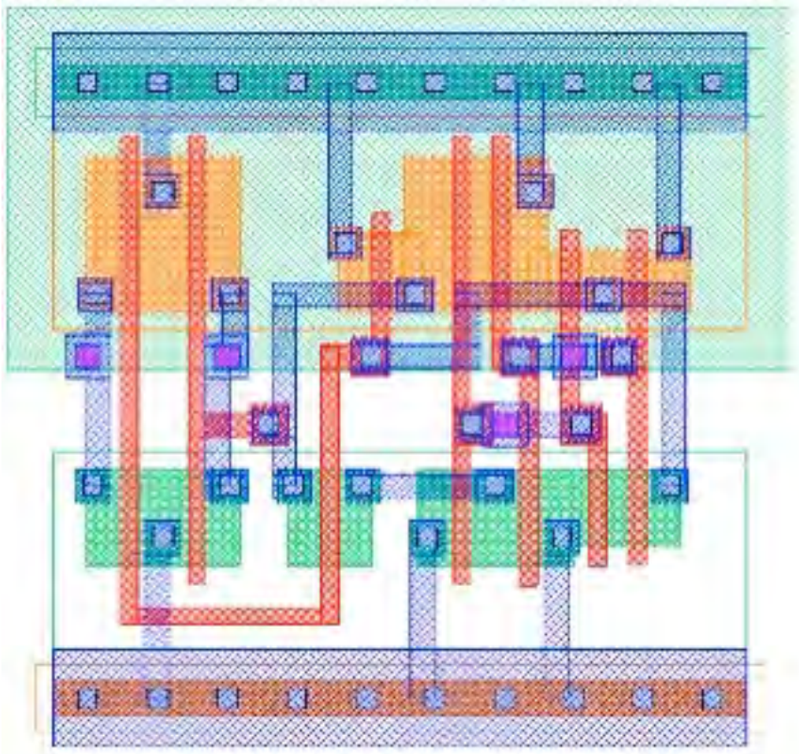
Many layout decisions can contribute to power reduction

Layout Generated Automatically with Parrot Tool Suite

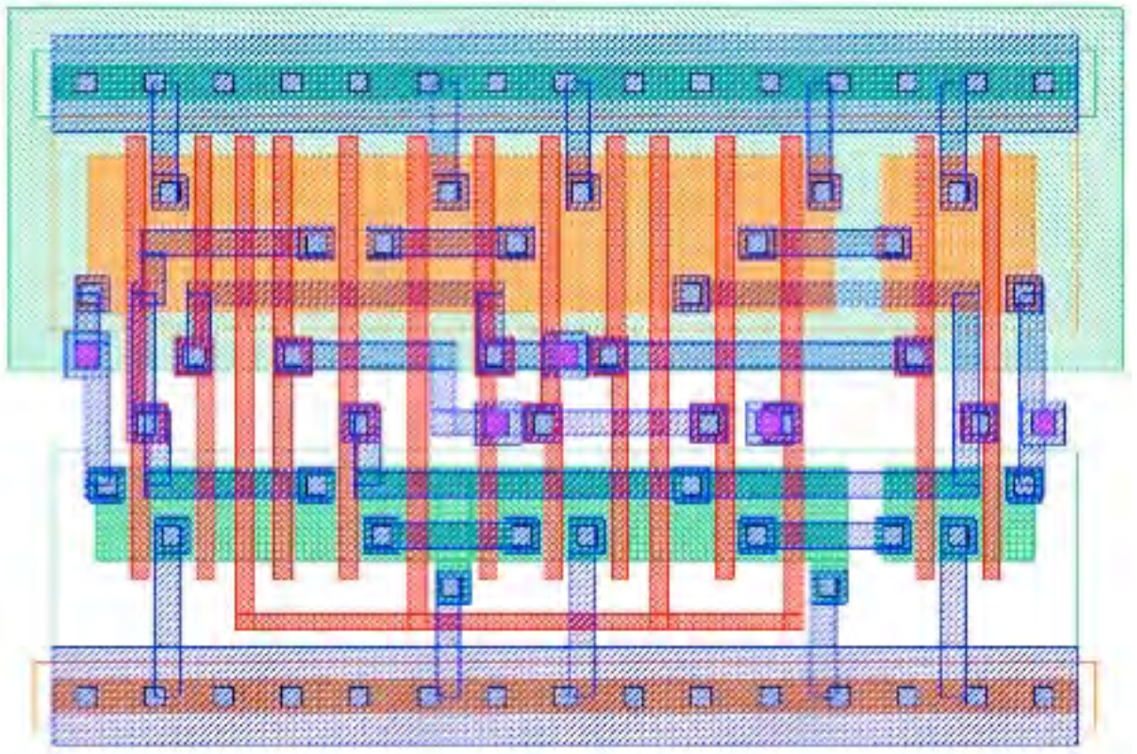


UFRGS

ASTRAN Layouts



ADD22



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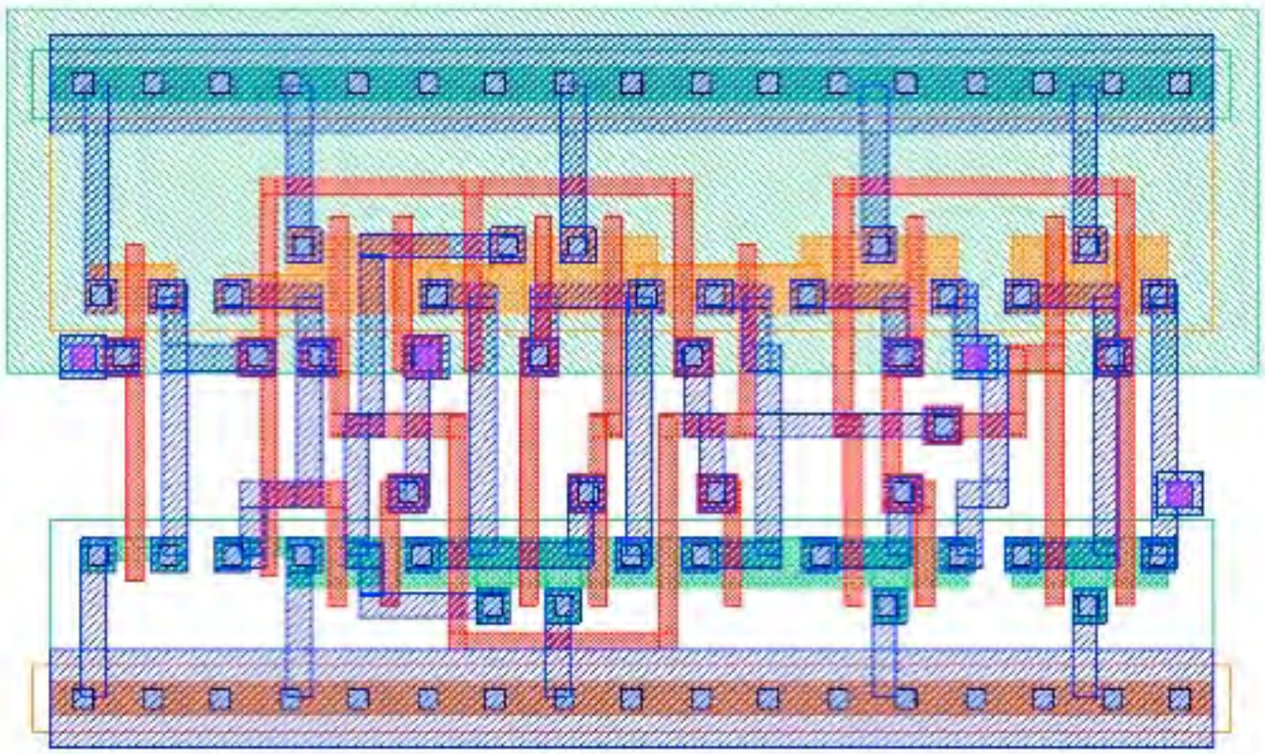
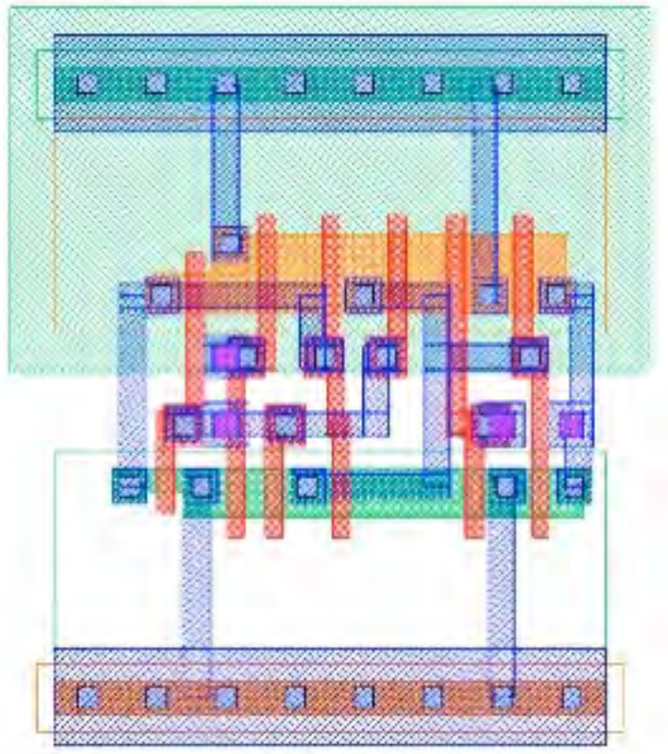
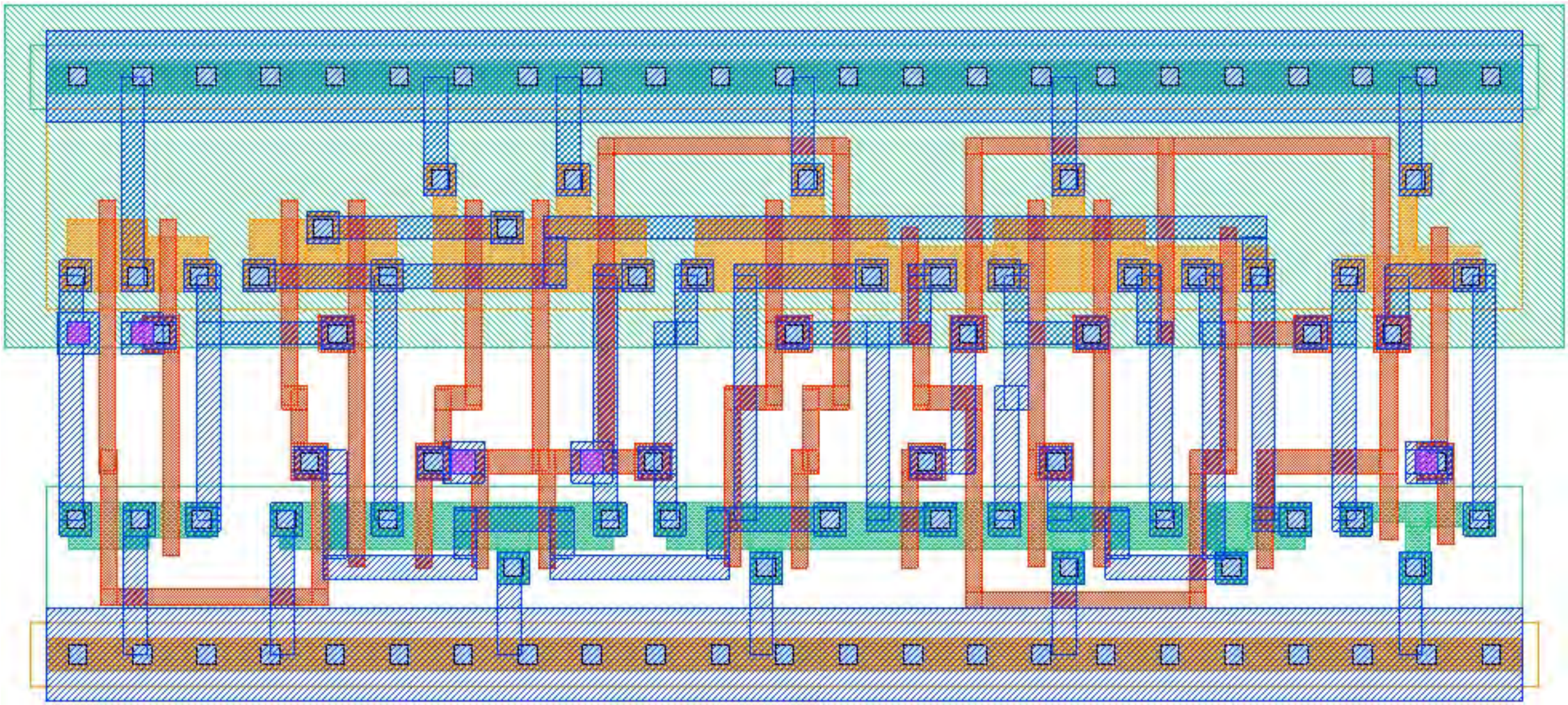


DF1



MUX21

ASTRAN Layouts

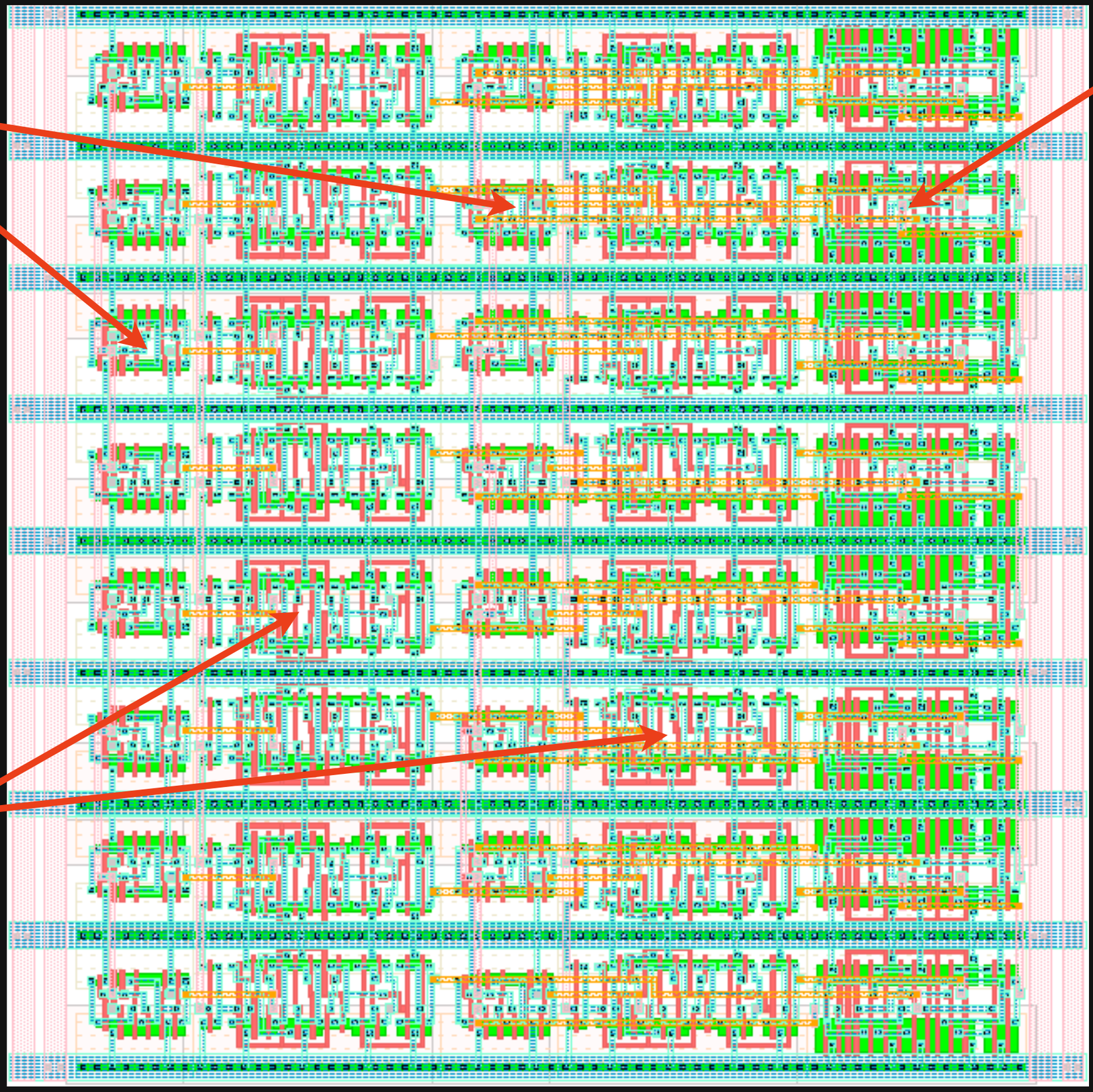


JK1 (34 transistors)

Adder

Adder

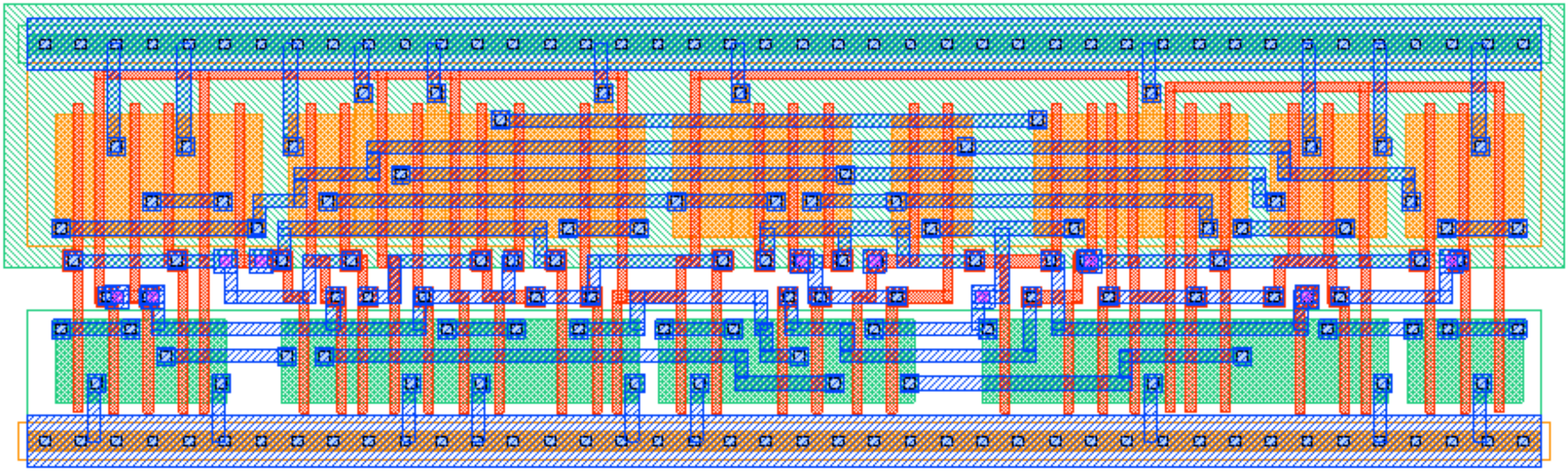
Mux



Register

ASTRAN Layouts

Non-Complementary Logic

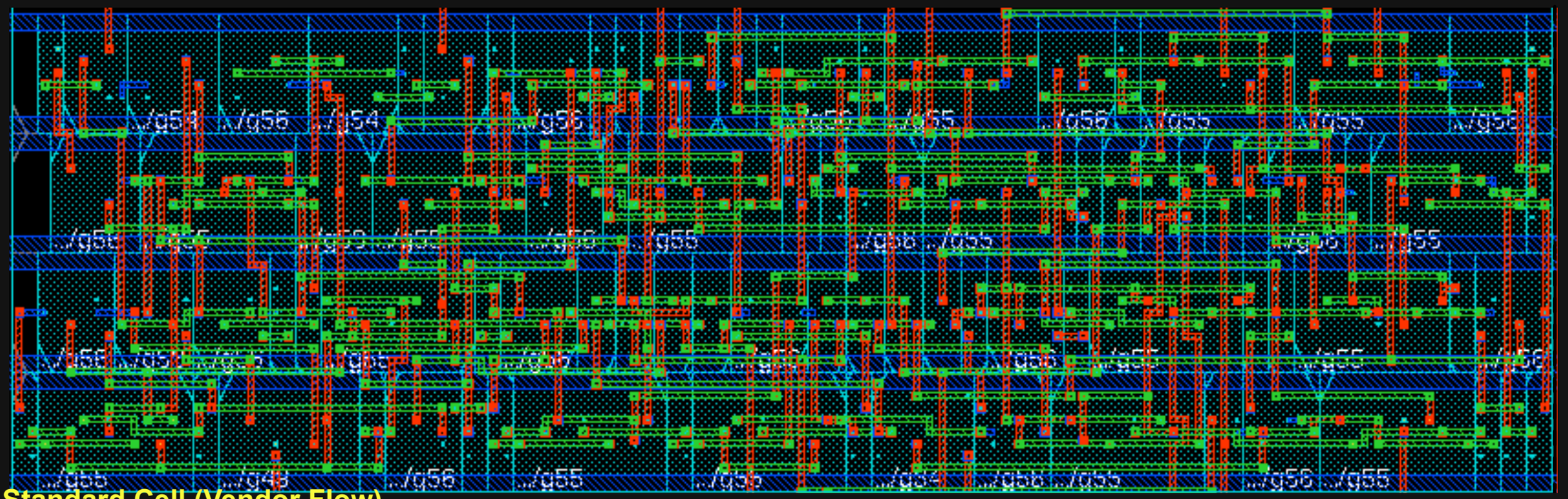


LBBDD_0117177F177F7FFF (68 transistors)

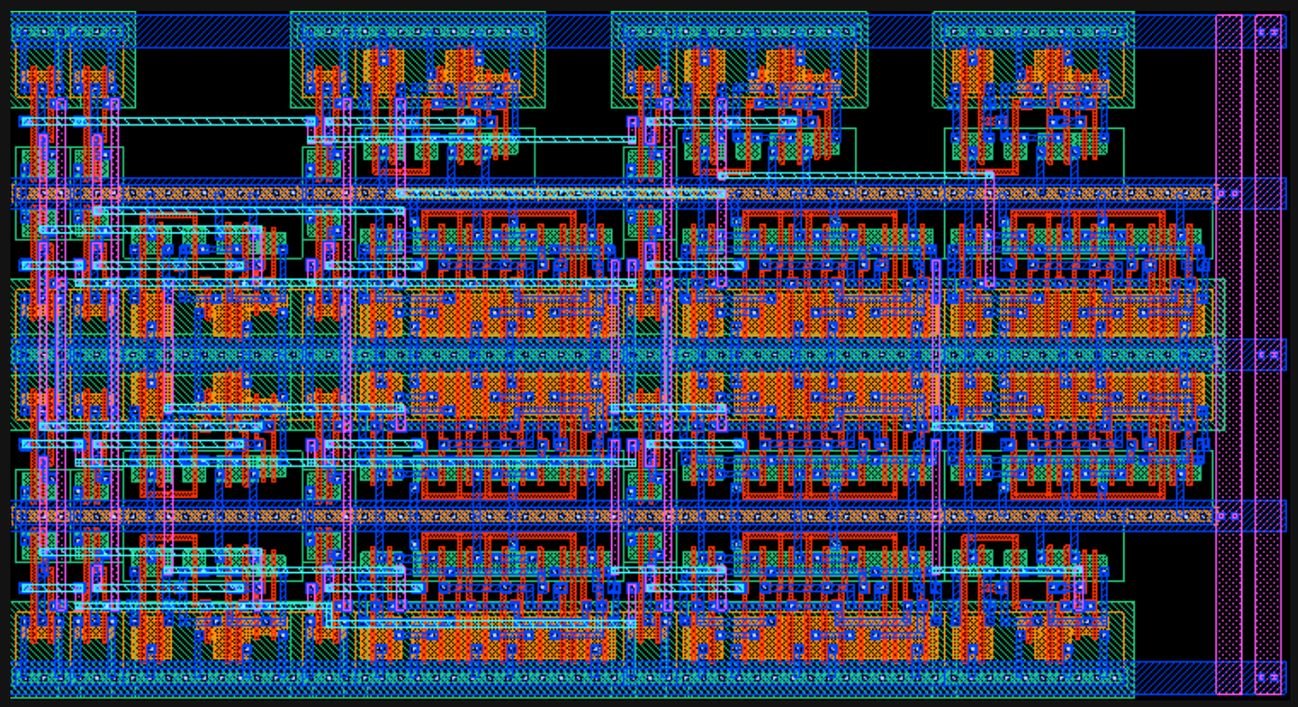
Runtime: 36 min

L.S.da Rosa Jr., F.Marques, T.M.G.Cardoso, R.P.Ribas, S.S.Sapatnekar, A.I.Reis, Fast Transistor Networks from BDDs. SBCCI 2006, pp. 137-142.

Multiplier Carry-Save 4x4



Standard Cell (Vendor Flow)

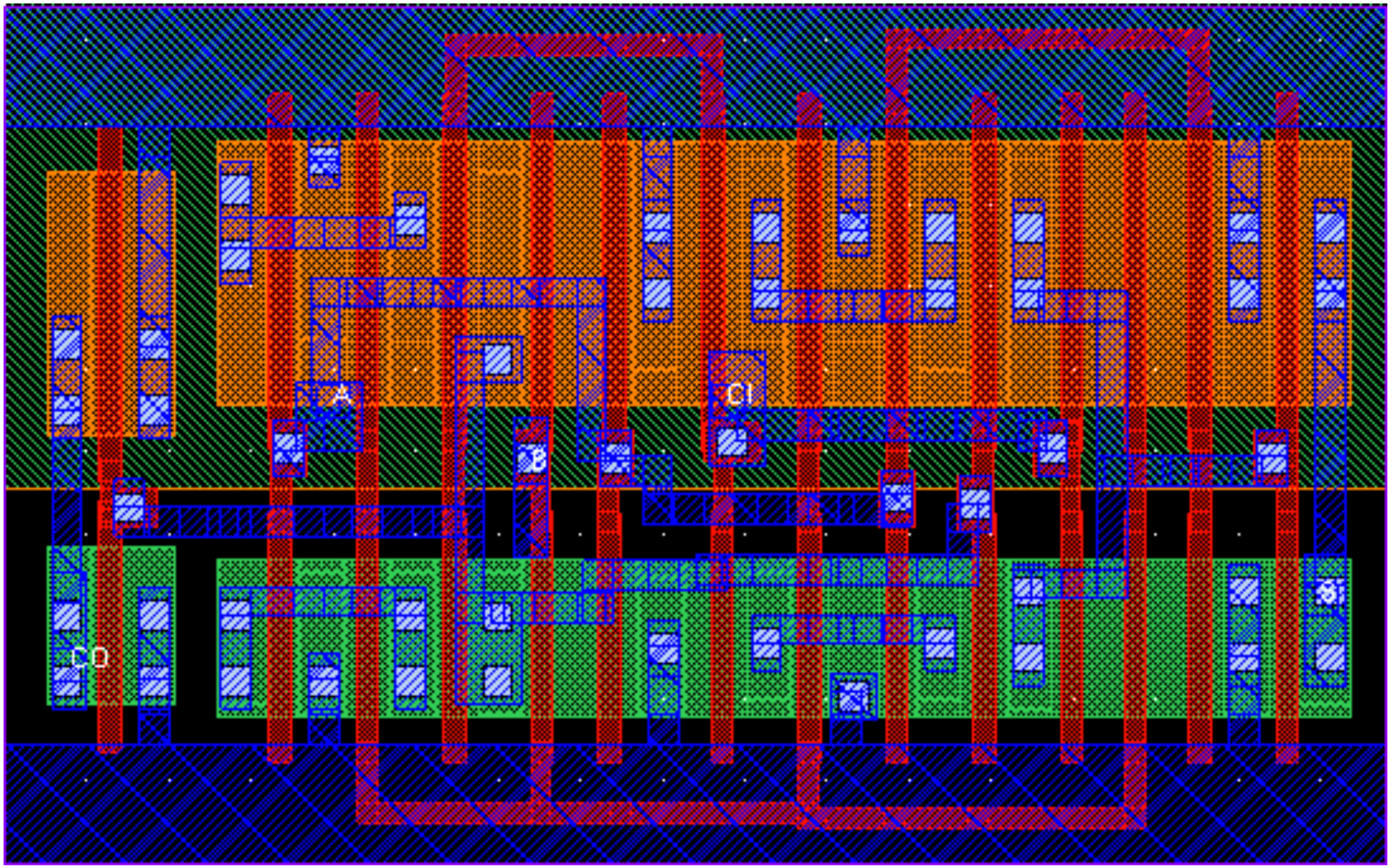


Generated with our Data Path Compiler

Multiplier Carry-Save 4x4

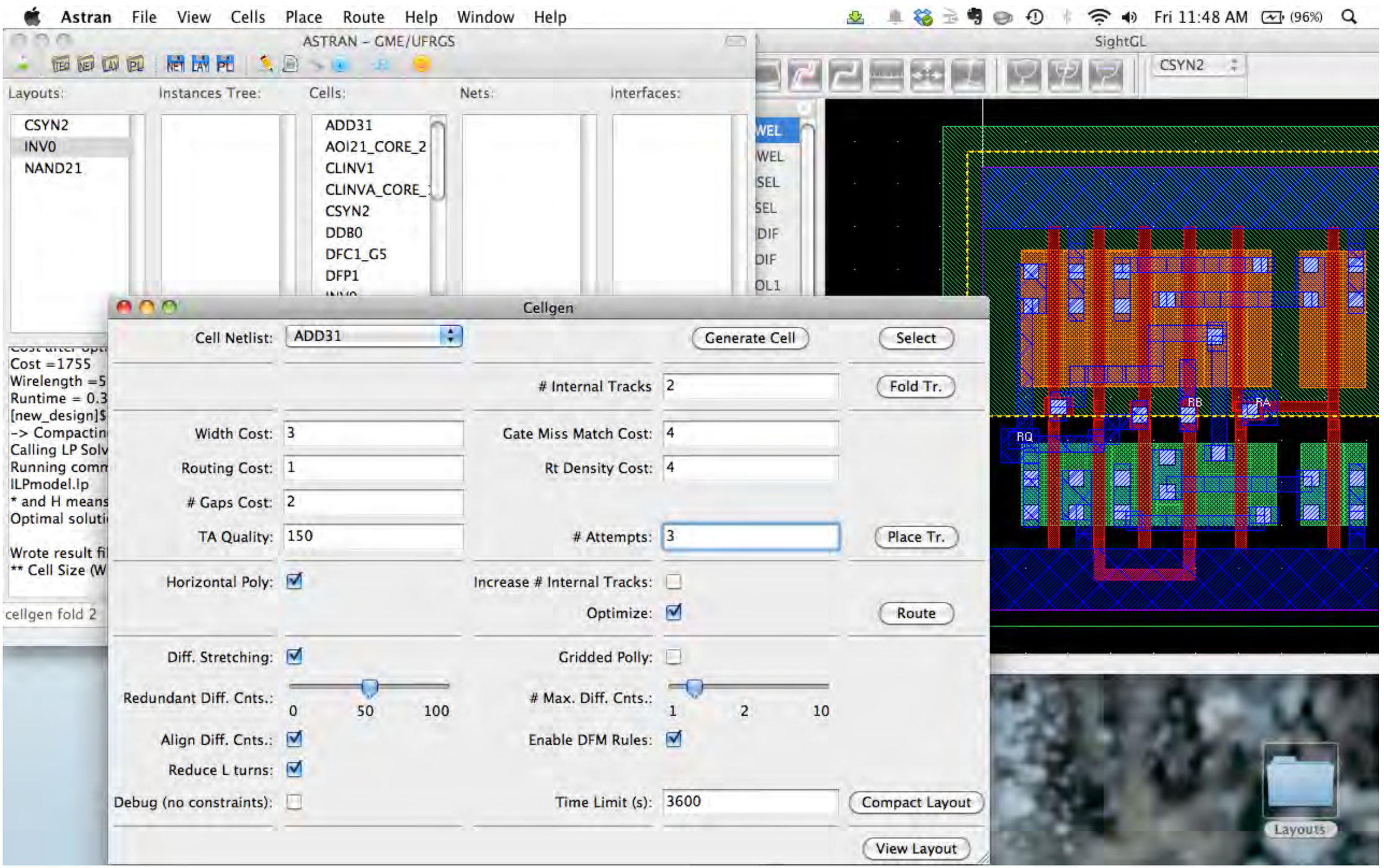
	Standard Cell	ASTRAN	Gain (%)
Number of Cells	52	28	46
Number of Transistors	634	376	59.3
Area (μm²)	6716	5070	24.5
Delay (ps)	2174	1896	12.8
Power (mW)	6.45	3.97	61.55

ASTRAN



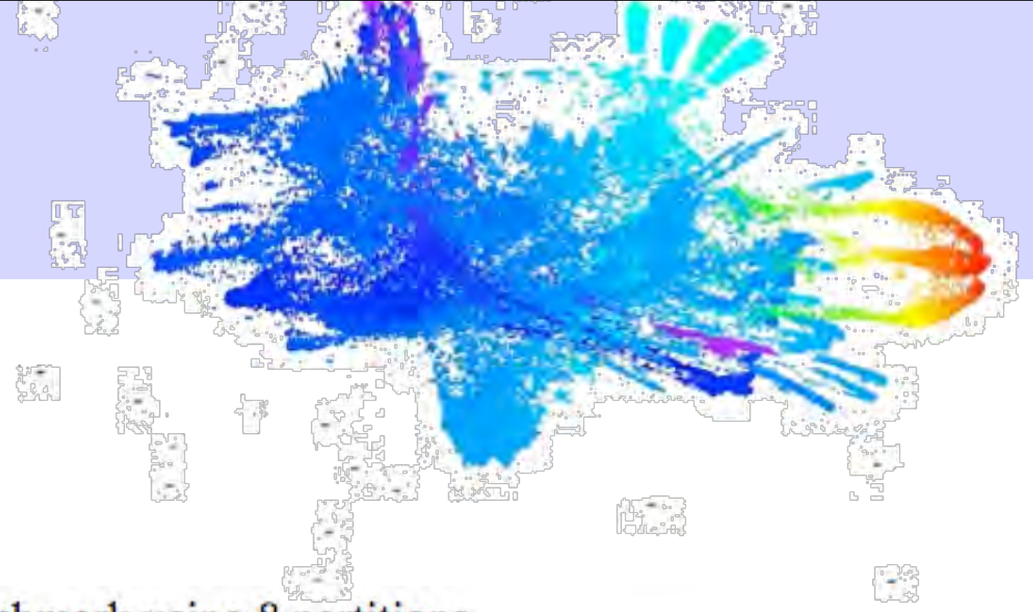
65 nm

ASTRAN

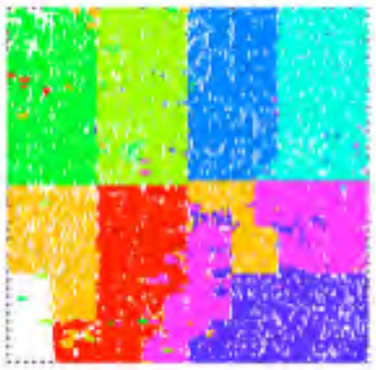
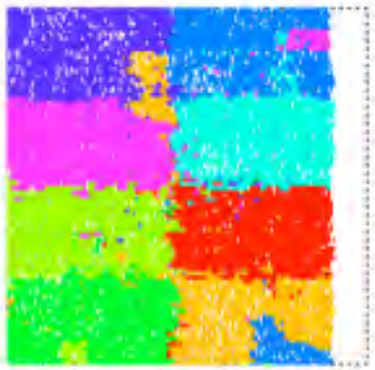

Astran File View Cells Place Route Help Window Help
Fri 11:48 AM (96%)
ASTRAN – GME/UFRGS
Layouts:
Instances Tree:
Cells:
Nets:
Interfaces:
CSYN2
INV0
NAND21
ADD31
AOI21_CORE_2
CLINV1
CLINVA_CORE_1
CSYN2
DDB0
DFC1_G5
DFP1
Cost =1755
Wirelength =5
Runtime = 0.3
[new_design]$
-> Compactin
Calling LP Solv
Running comm
ILPmodel.lp
* and H means
Optimal soluti
Wrote result fi
** Cell Size (W
cellgen fold 2
Cellgen
Cell Netlist: ADD31
Generate Cell
Select
Internal Tracks 2
Fold Tr.
Width Cost: 3
Gate Miss Match Cost: 4
Routing Cost: 1
Rt Density Cost: 4
Gaps Cost: 2
TA Quality: 150
Attempts: 3
Place Tr.
Horizontal Poly:
Increase # Internal Tracks:
Optimize:
Route
Diff. Stretching:
Gridded Polly:
Redundant Diff. Cnts.: 0 50 100
Max. Diff. Cnts.: 1 2 10
Align Diff. Cnts.:
Enable DFM Rules:
Reduce L turns:
Debug (no constraints):
Time Limit (s): 3600
Compact Layout
View Layout
SightGL
CSYN2
RB
RA
RQ
Layouts

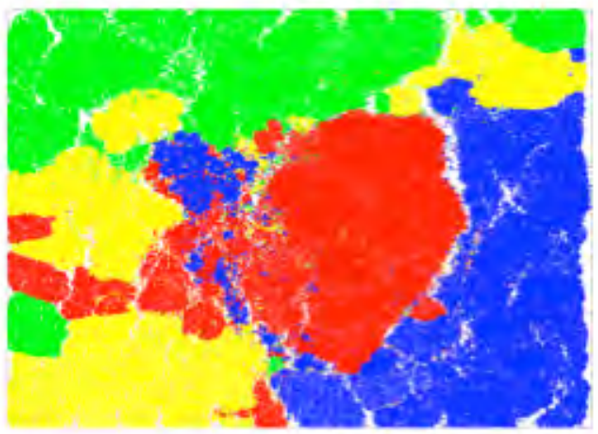
Visualization Tools

More on colors…

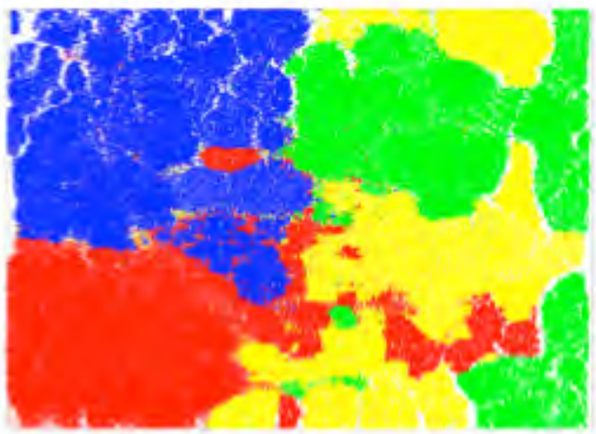


Tab.1 - Min-Cut coloring scheme. Images for ibm01 benchmark using 8 partitions.

Capo	Dragon	FastPlace 3	mPL
HPWL: 1.90689e+06	HPWL: 1.87986e+06	HPWL: 1.72773e+06	HPWL: 1.6185e+06
			



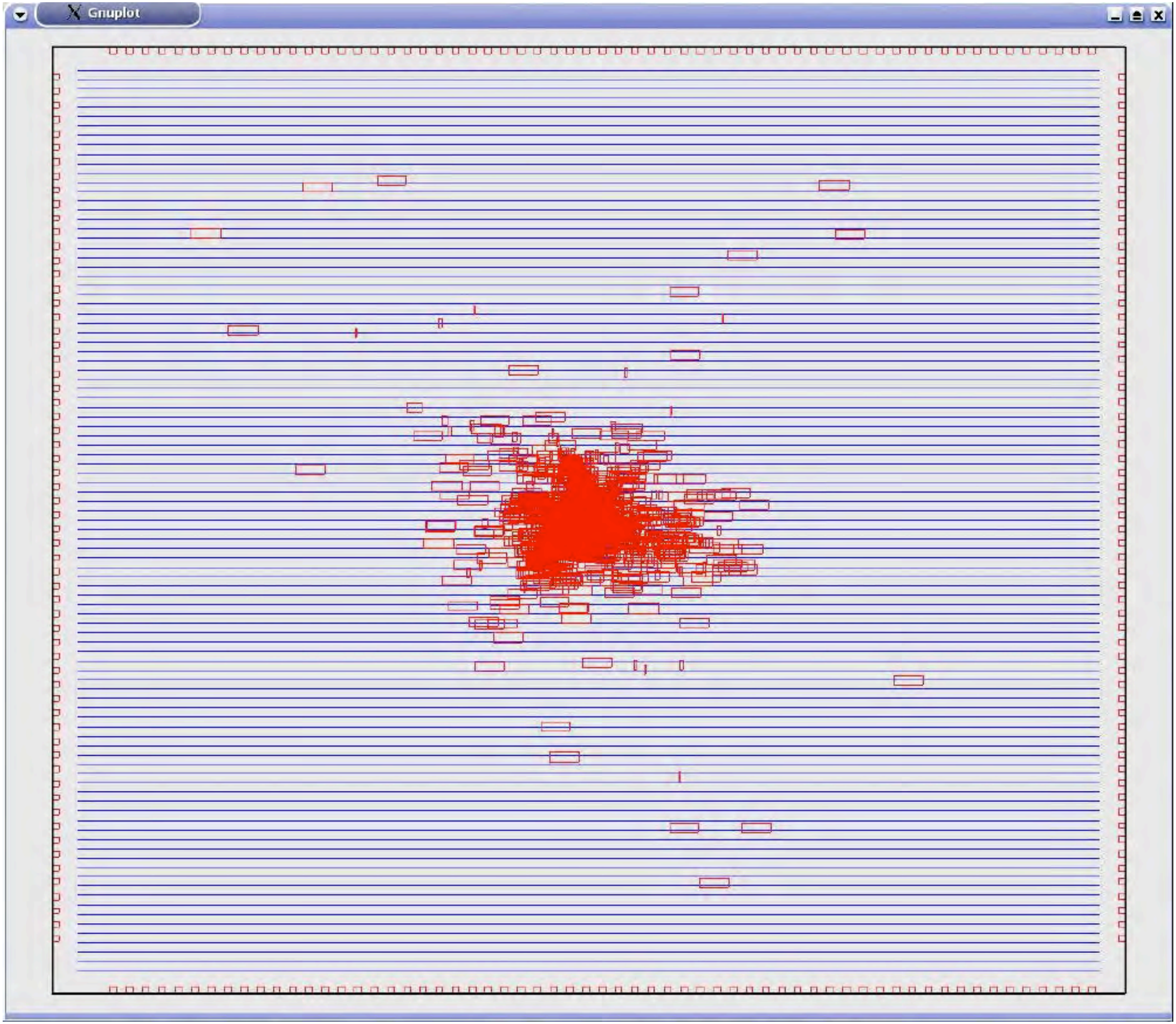
(a)

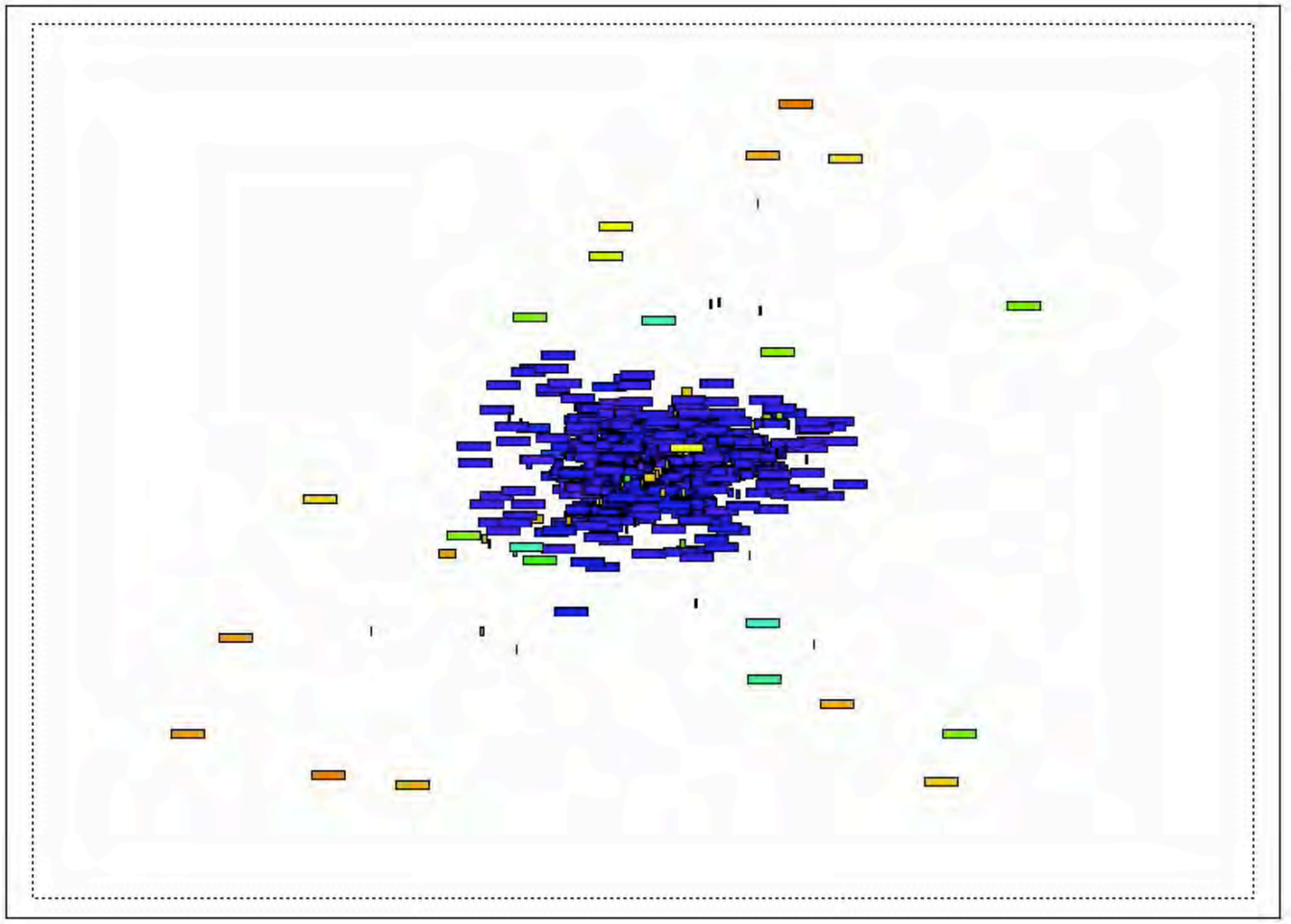


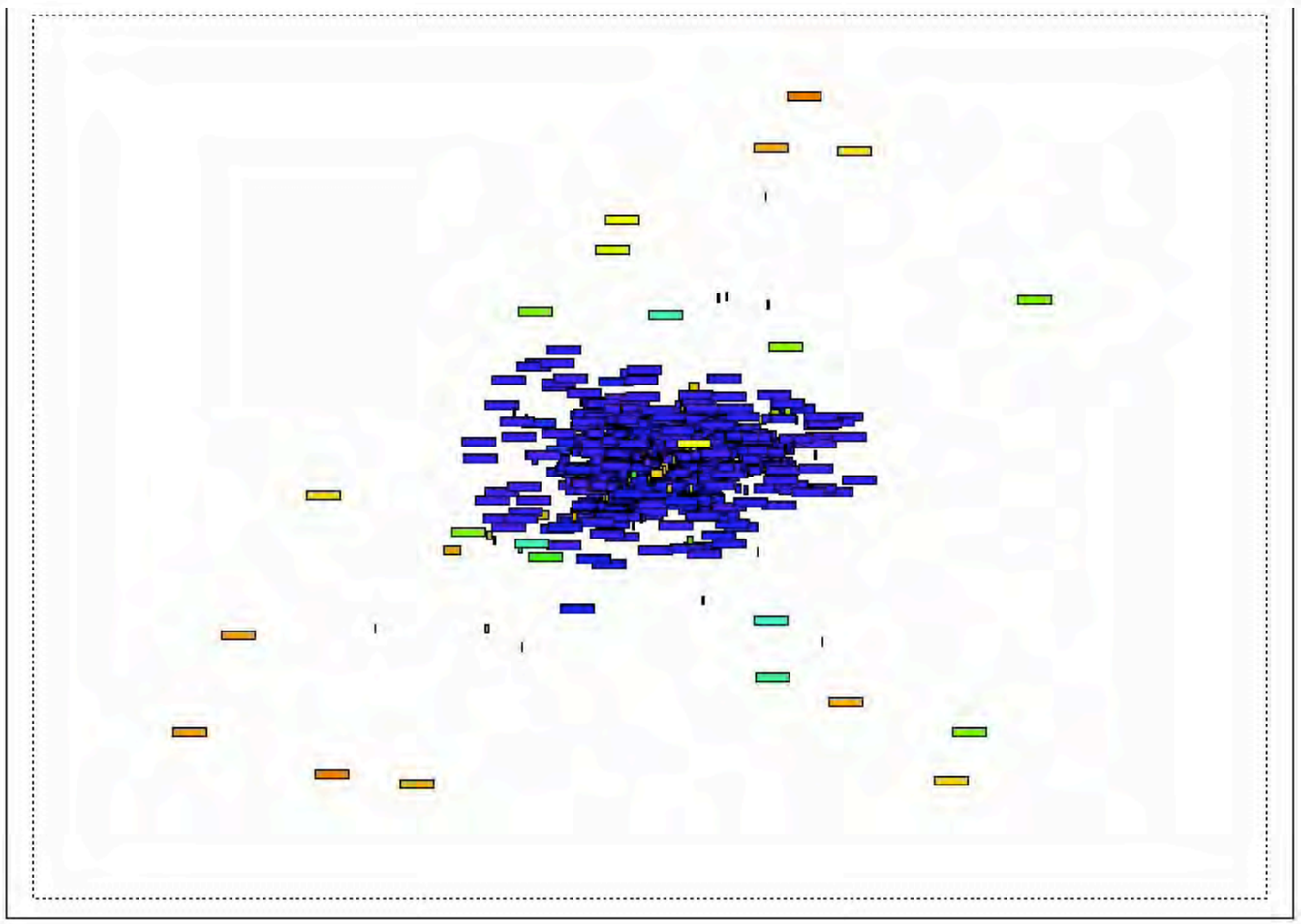
(b)

(c)

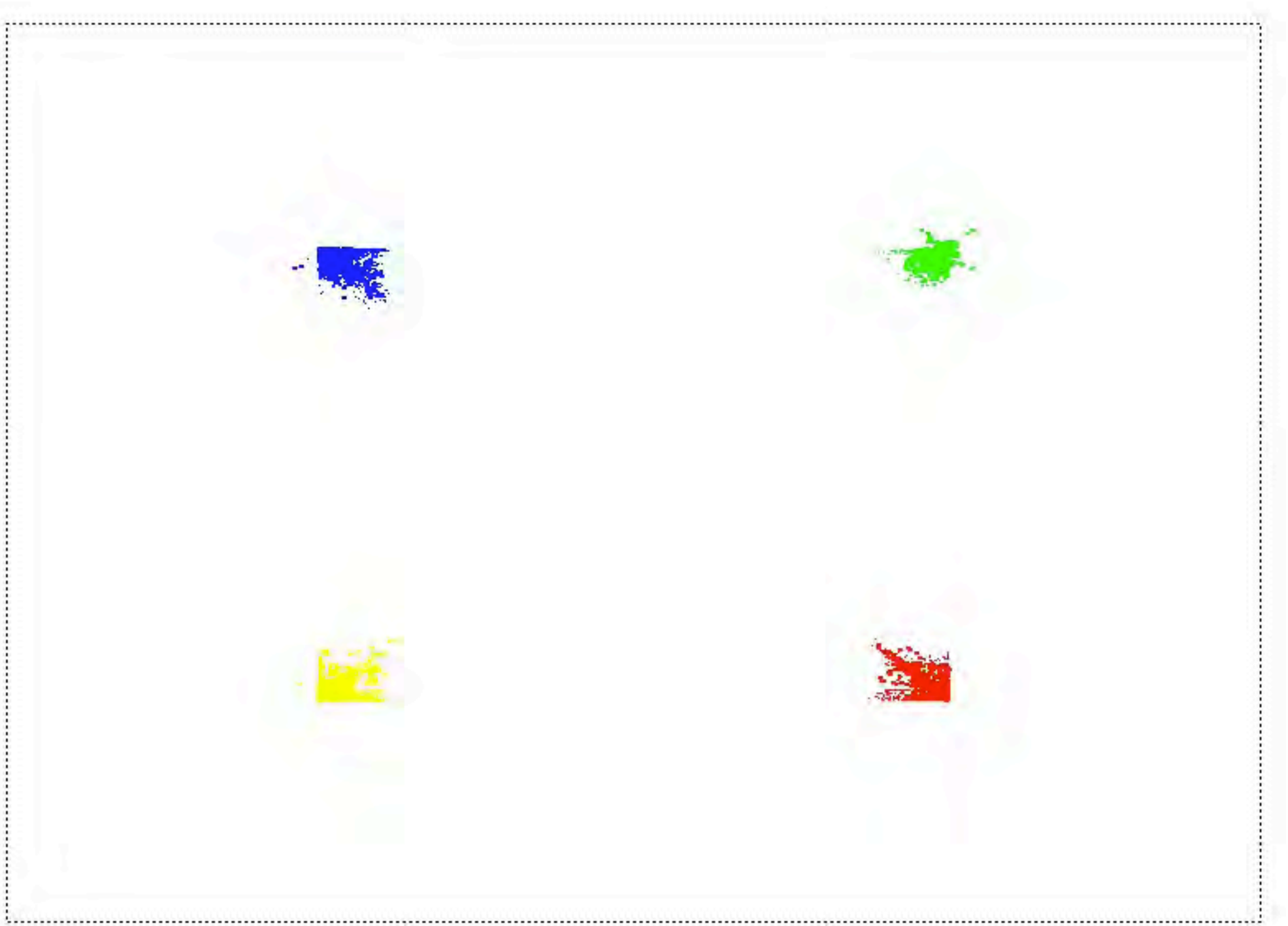
Fig. 3 – Placement coloring. (a) Our prior placer result; (b) FastPlace 3 result; (c) Our final placer result using partitioning for initial placement.


Gnuplot



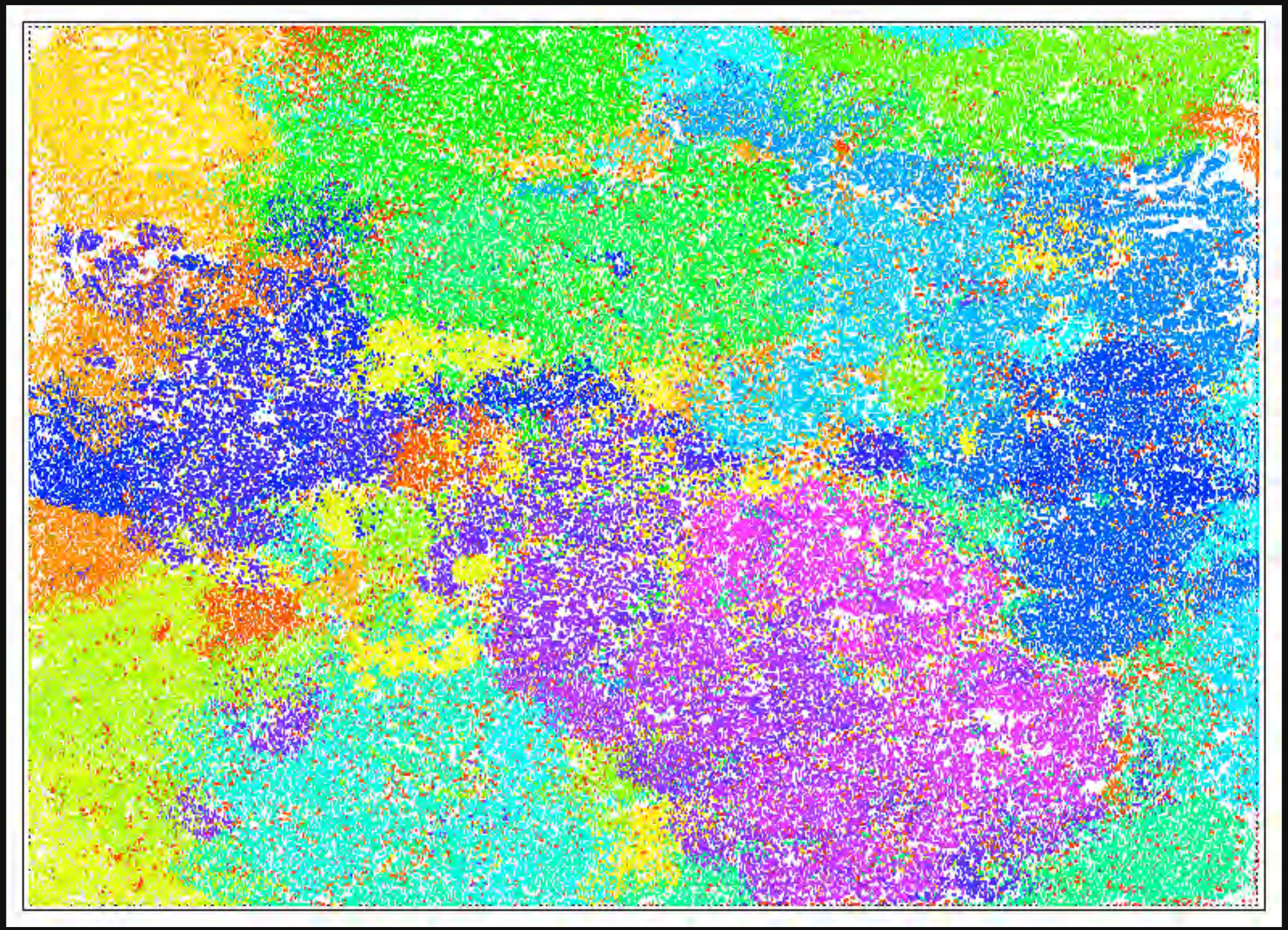


Placement using PlaceDL



Placement of the IBM18 circuit using UFRGS tools

> 200 thousand logic cells

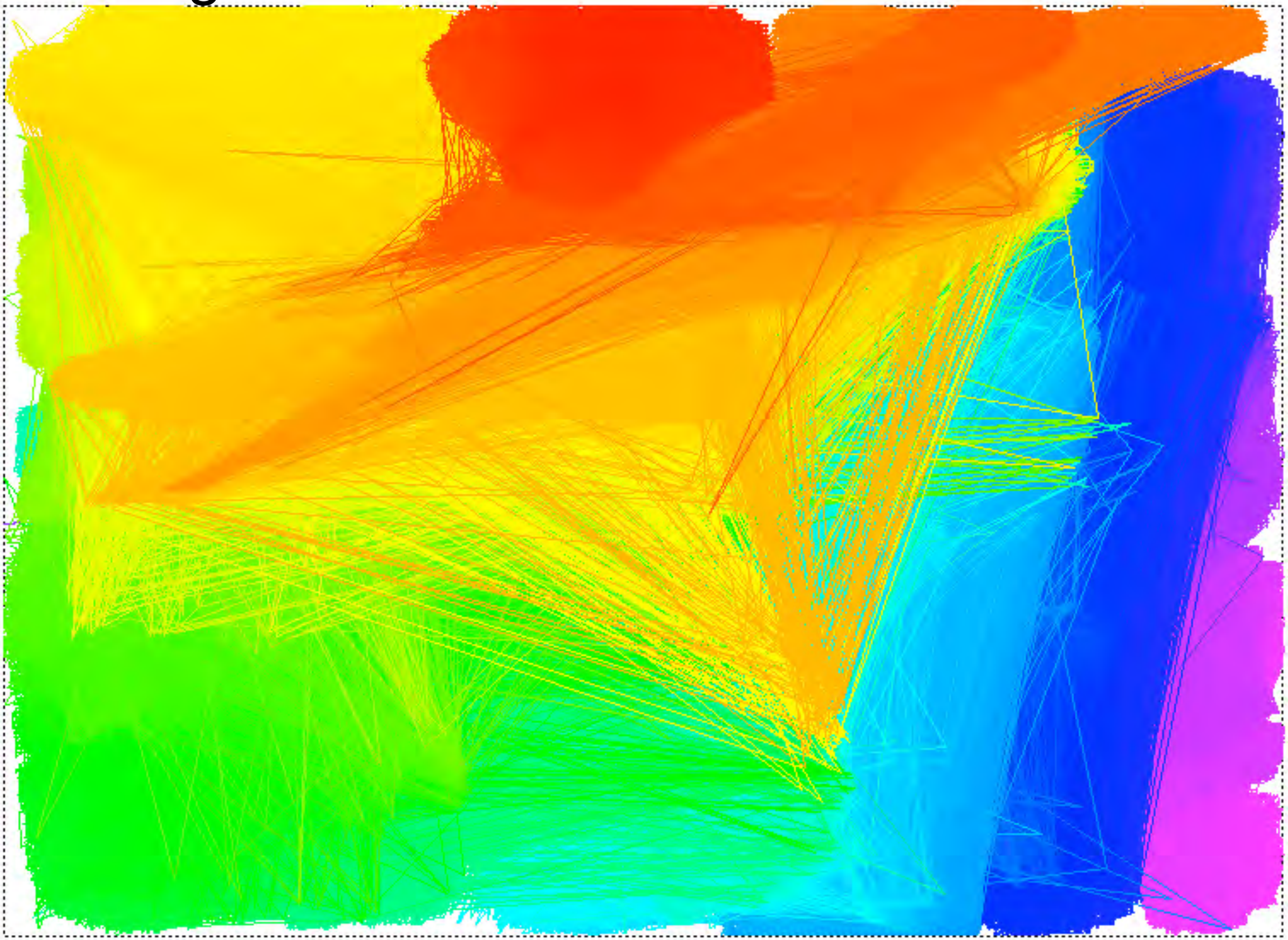


Routing Colors

IBM

Routing Colors

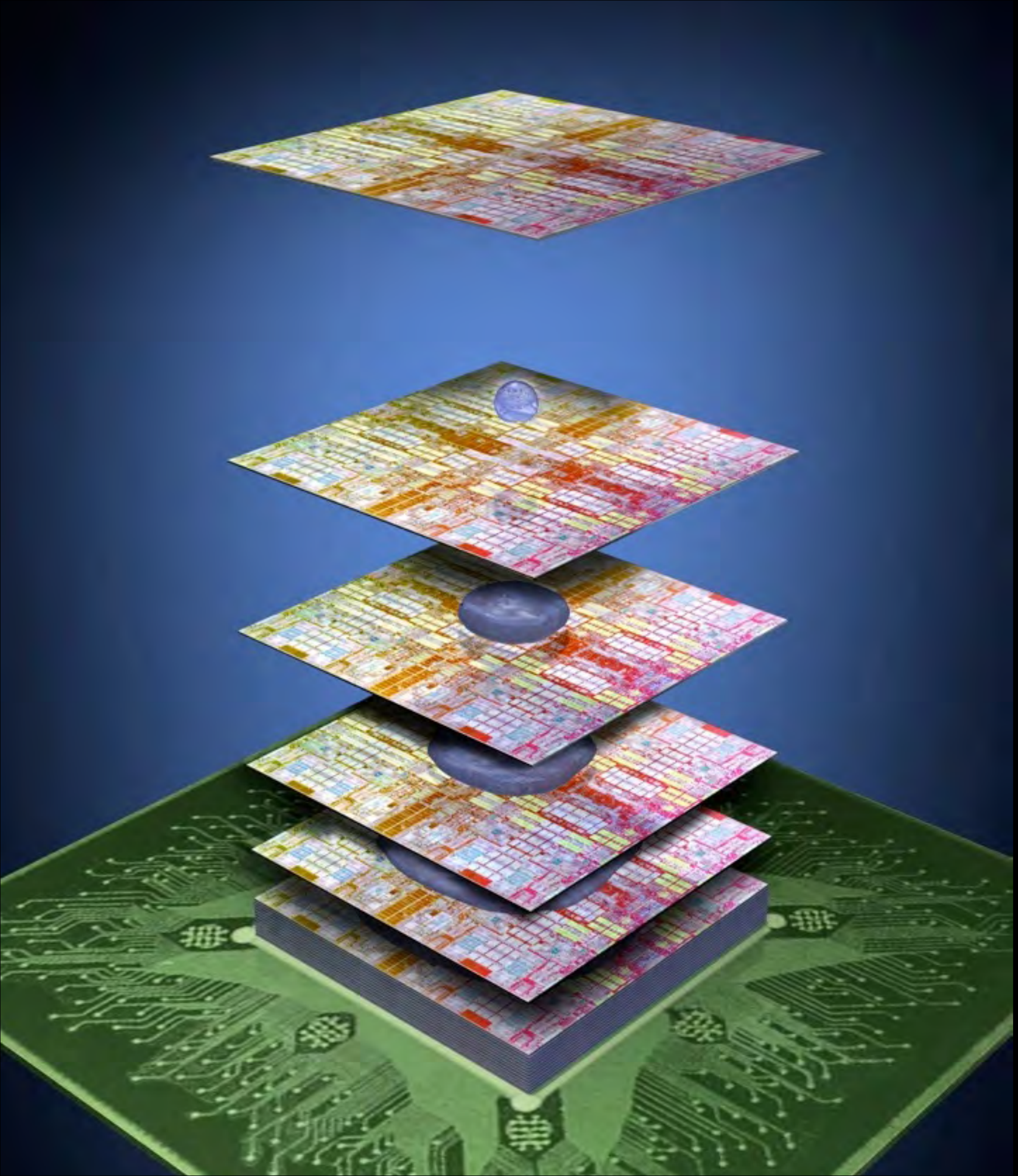
IBM18



EDA

Tools Running on FPGAs

3D chips



fonte: IBM

Conclusions

more
&
more

green
chips

Power
Optimization
in all abstraction levels

Conclusions

In NanoCMOS a way to reduce Power Consumption is to reduce the amount of transistors

Conclusions

Optimization on the Number of Transistors allows:

Area reduction

Reduction on the number of transistors

Cell library free

Wirelength minimization

Delay Reduction

Power Reduction

Conclusions

Let's do

Transistor Level

Design Automation

to reduce the amount of transistors

and POWER CONSUMPTION

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Optimization is the Keyword in NanoCMOs

Ricardo Reis

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