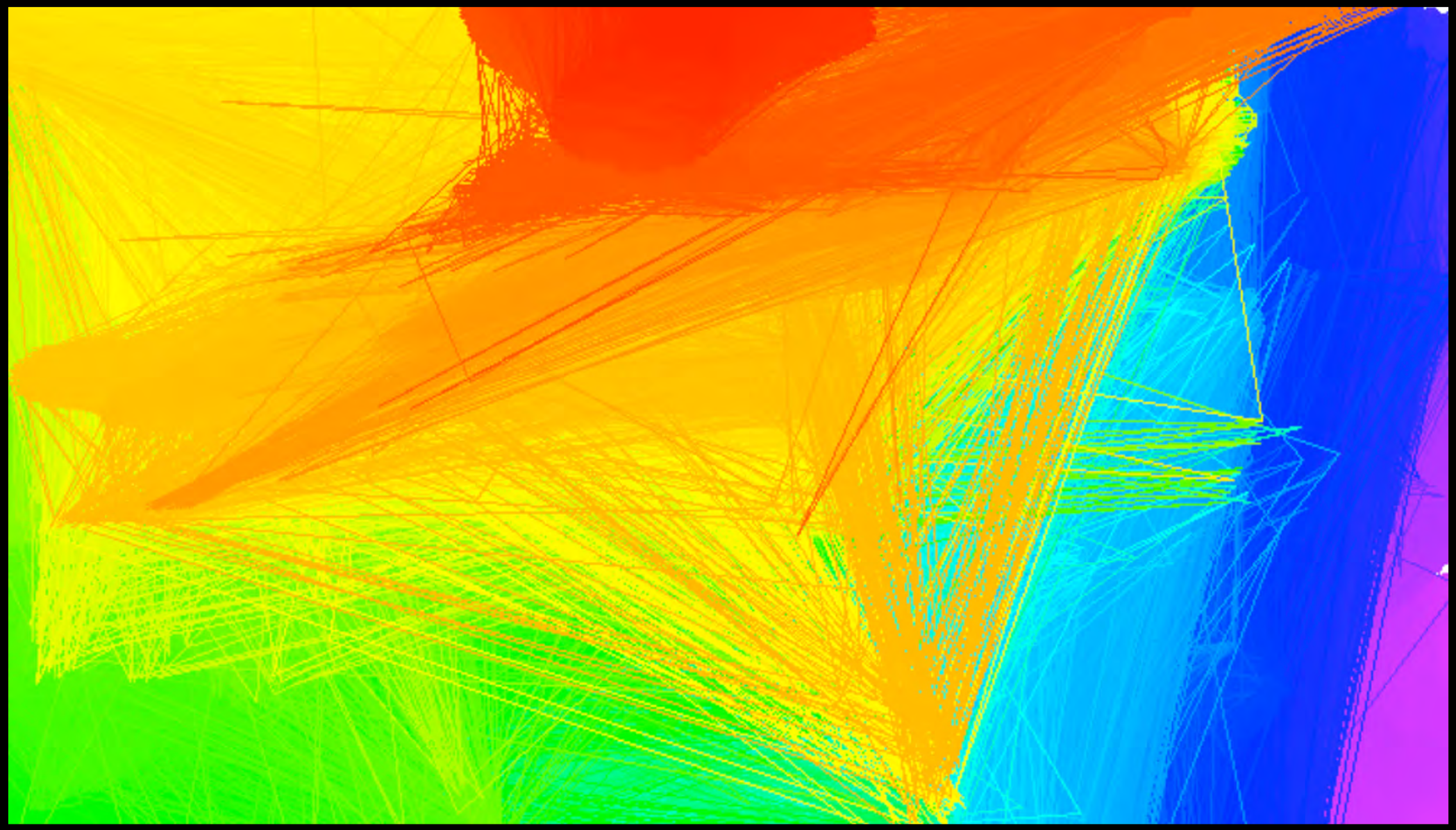


Visualization Tools

Ricardo Reis, Mateus Fogaça, Guilherme Flach

UFRGS

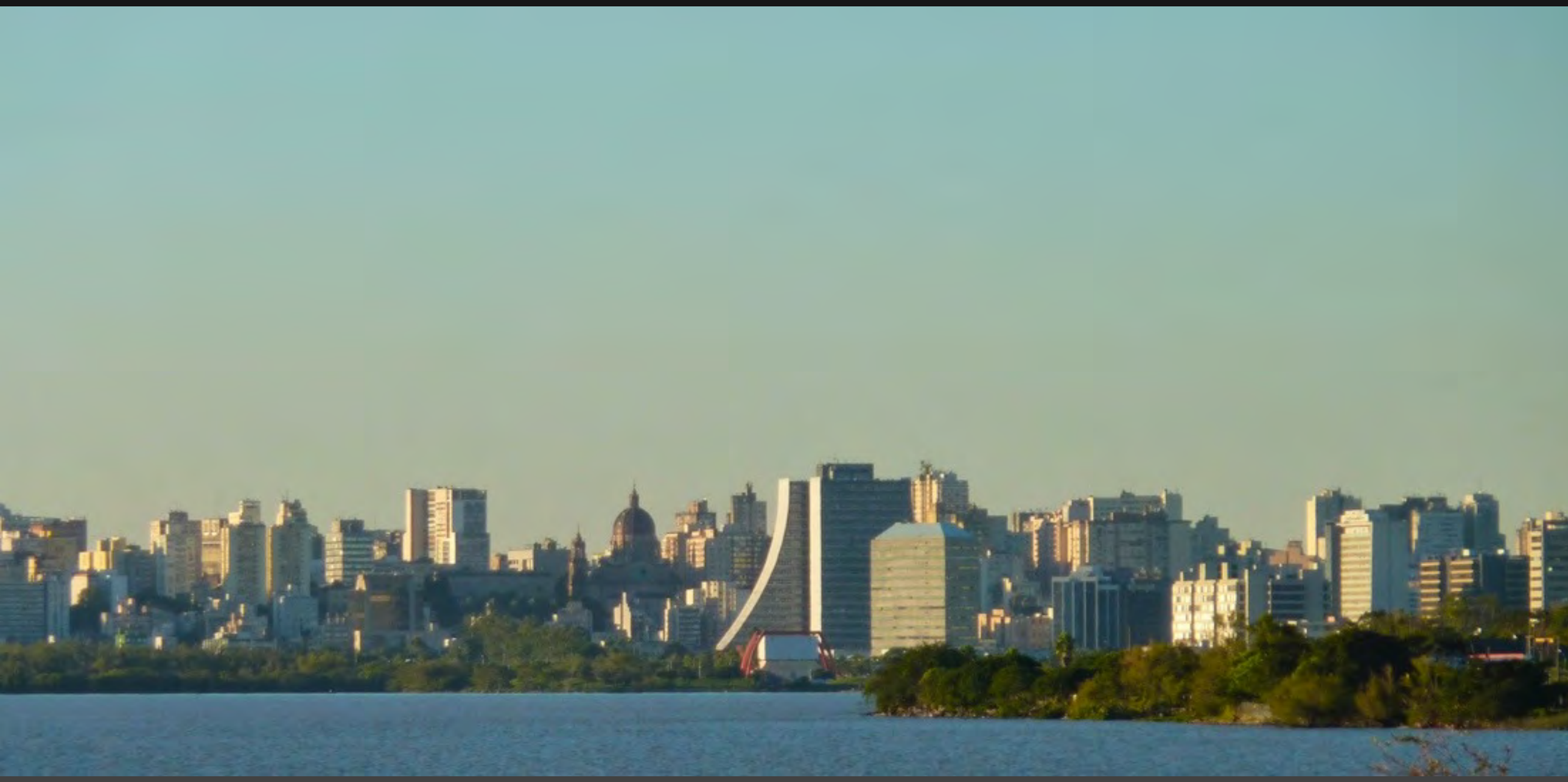
Where

do we come from ...

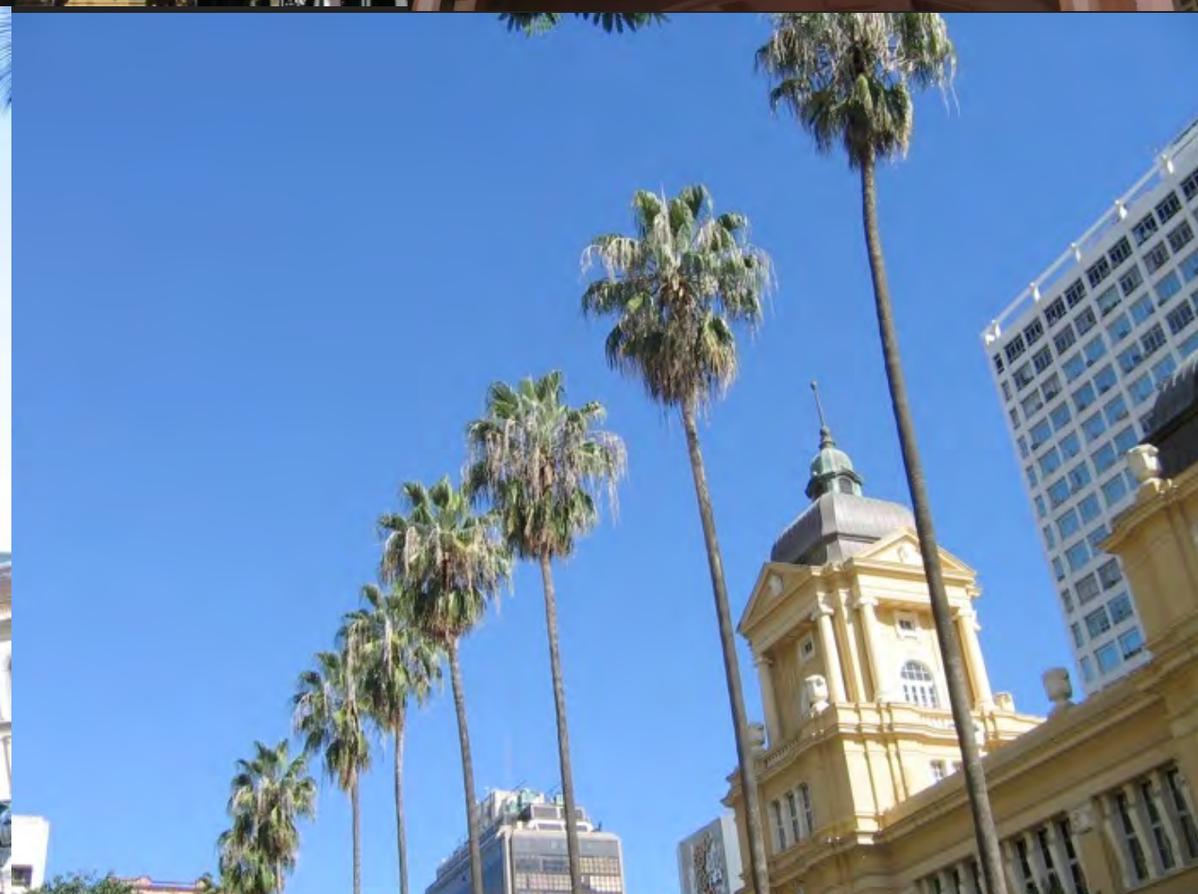

Porto Alegre

Where do we come from

Porto Alegre

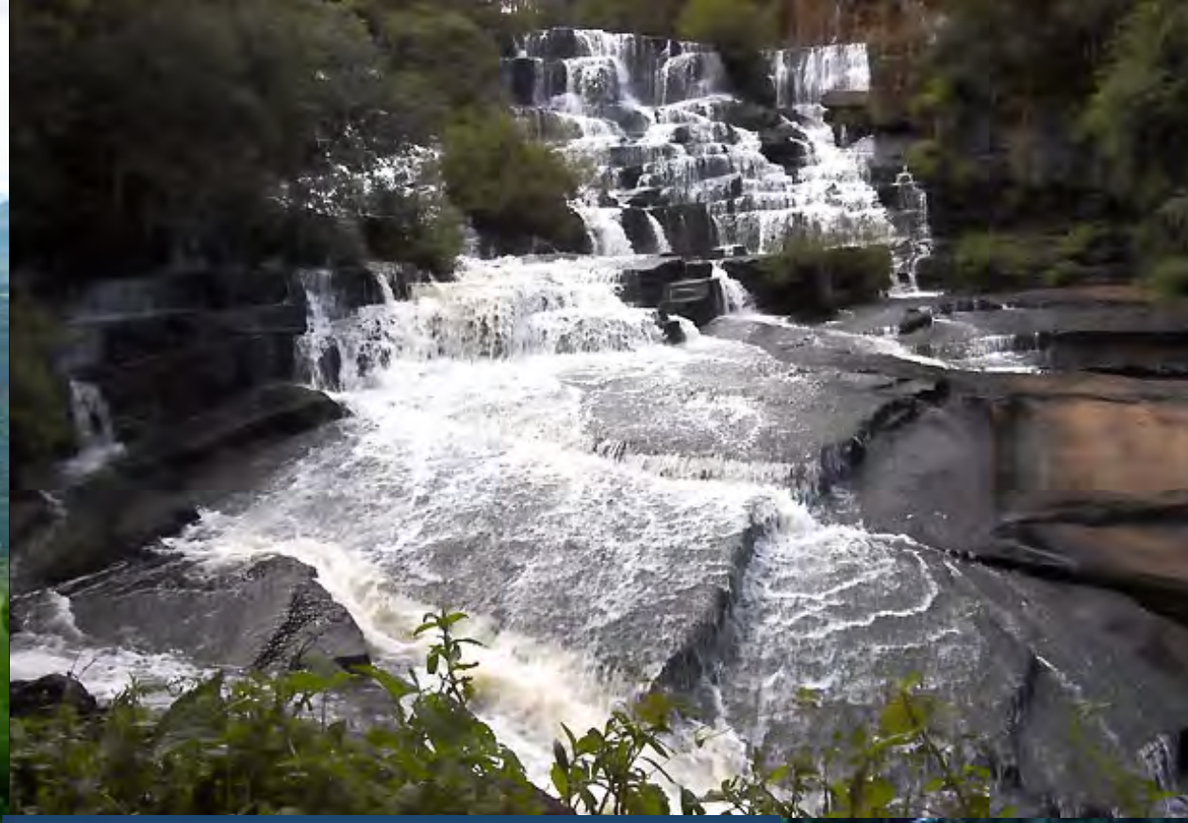


Porto Alegre



Ibere Camargo Museum

Porto Alegre



Instituto de Informática

CEITEC

Design Center - Administrative Building:

Design Center
Process Engineering
Adm. Offices
Teaching Rooms
Auditorium
5.100 m²

Manufacturing Building

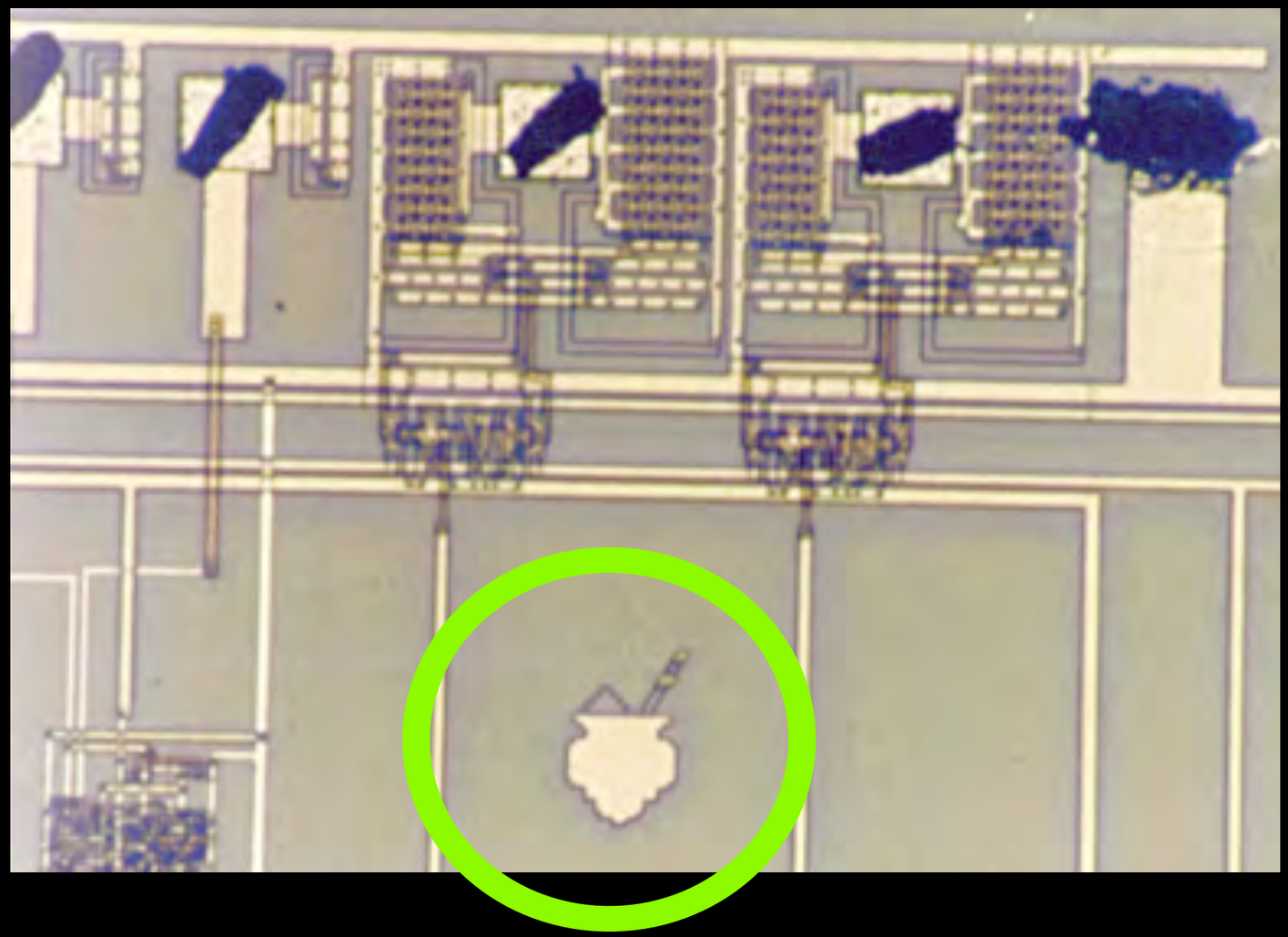
Manufacturing Cleanroom
Research & Development Cleanroom
Facilities and Support
9.600 m²

4.000 wafers/month (200 a 15.000 chips/ wafers)

CEITEC

A bit of History

1984 – Access to MPW prototyping (fabricated at ES2, France)

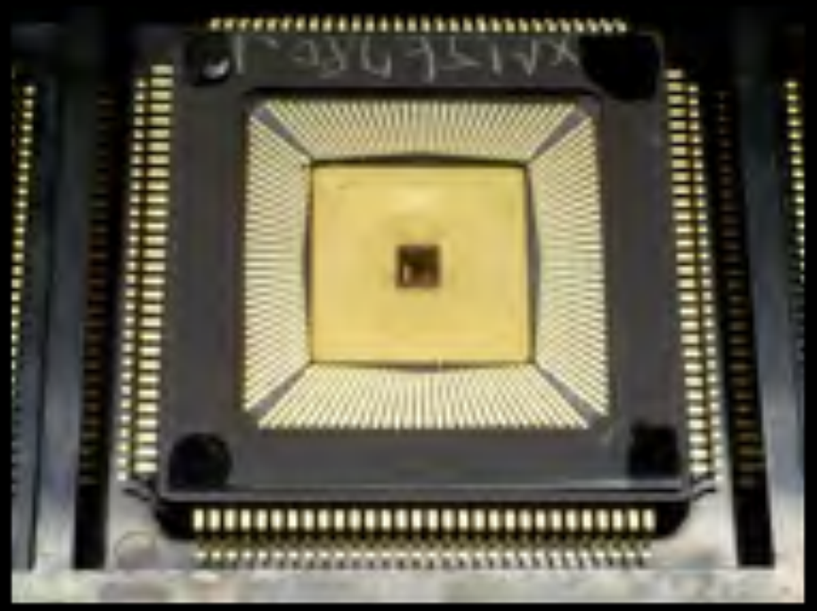


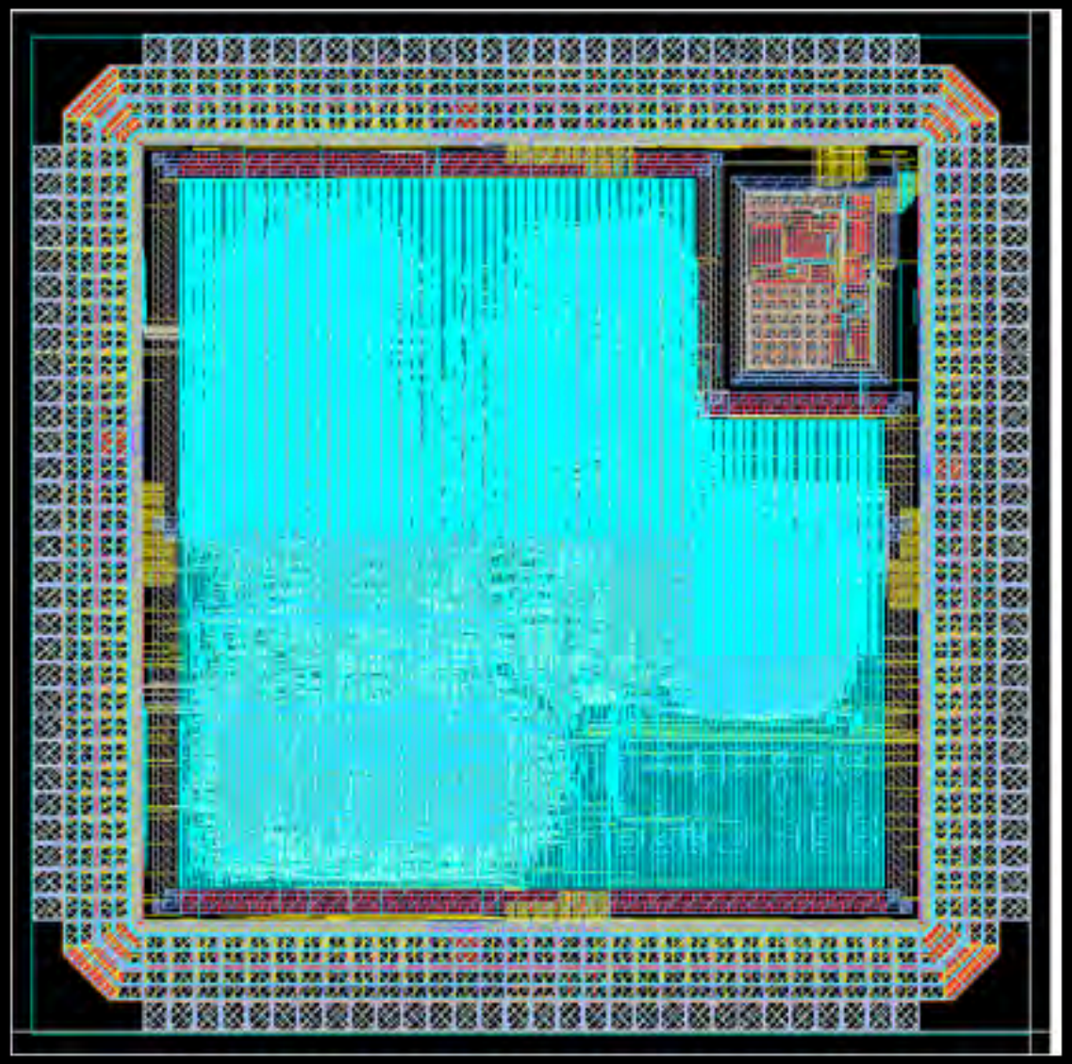
1986 – RISCO 16b/32b completed
First RISC Microprocessor in Brazil (Architecture to Layout)

2012

TMR MIPS Duo Core 32 bits

chip tolerant radiation effects

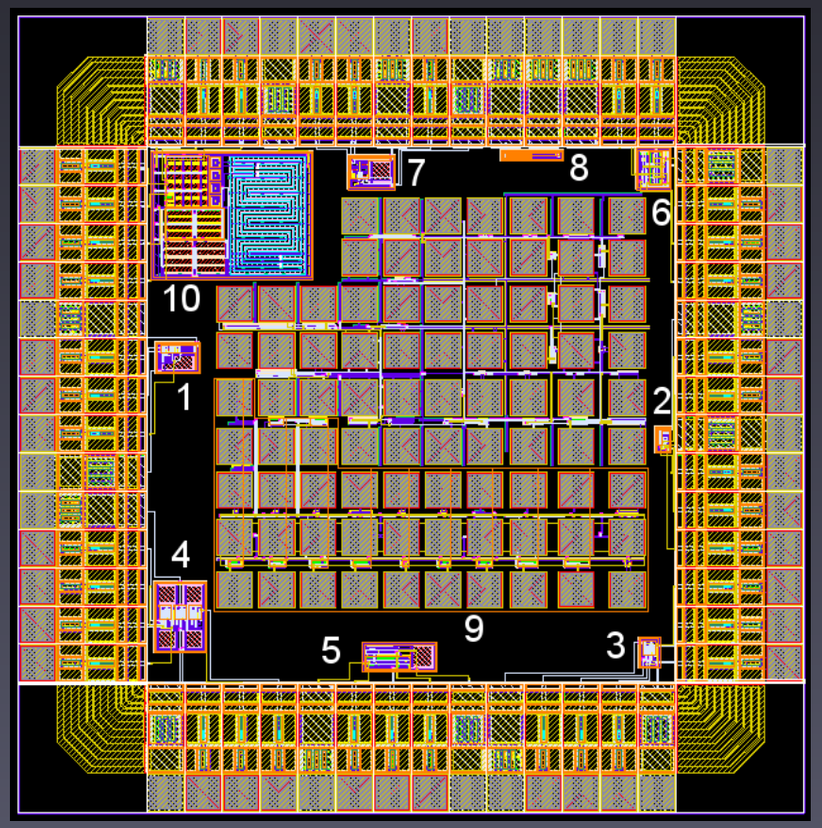


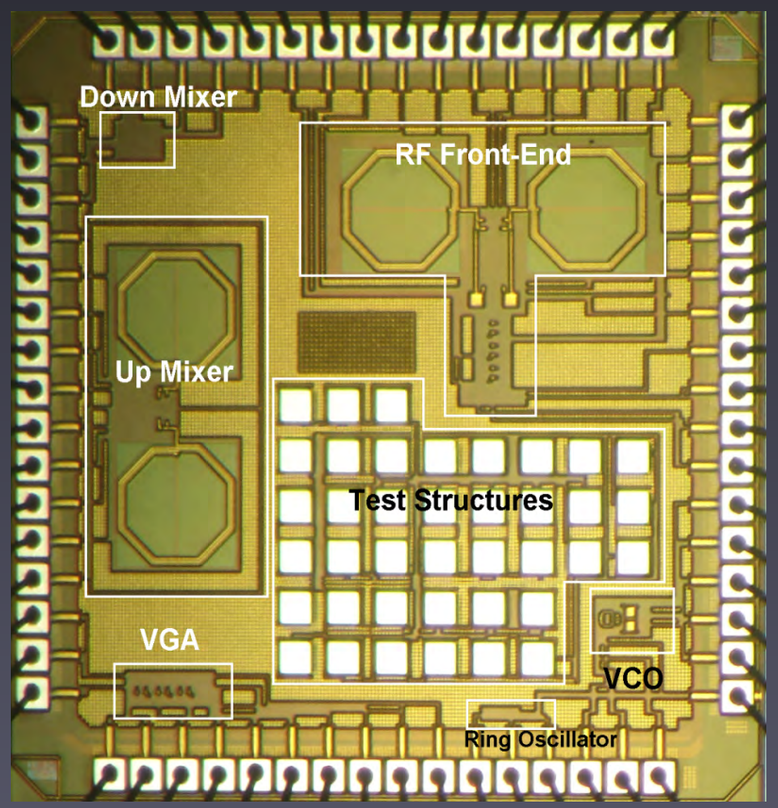


see more at: http://www.nscad.org.br/site/nsc21101

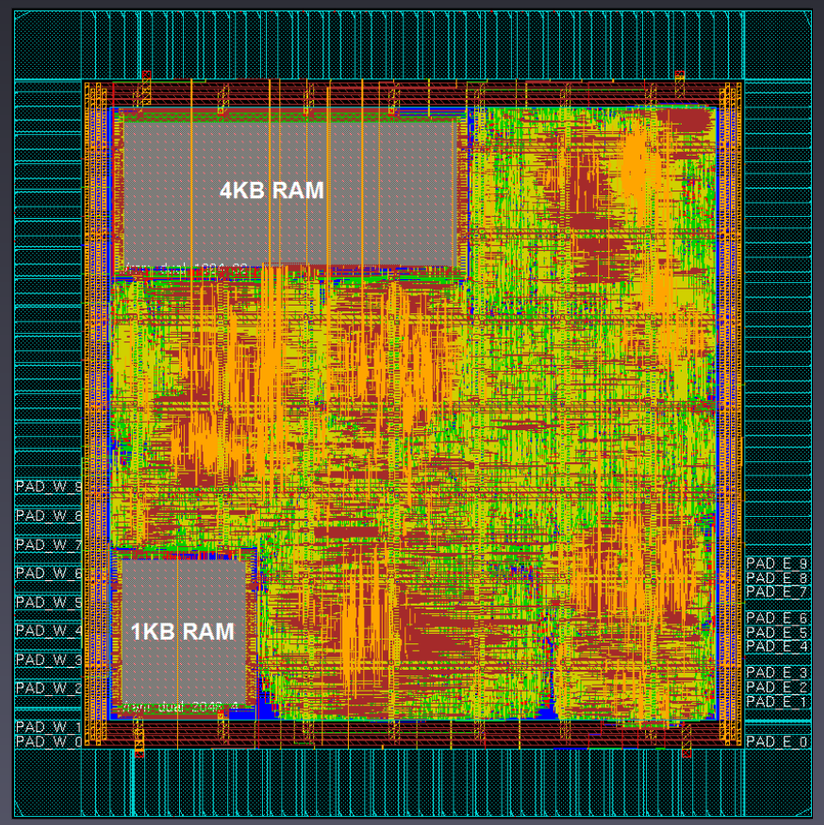
Microelectronics Group Research Topics

- Embedded Systems
- Analog Design
- Digital Design
- Design Methodologies
- VLSI Architectures and Dedicated Architectures
- Digital TV





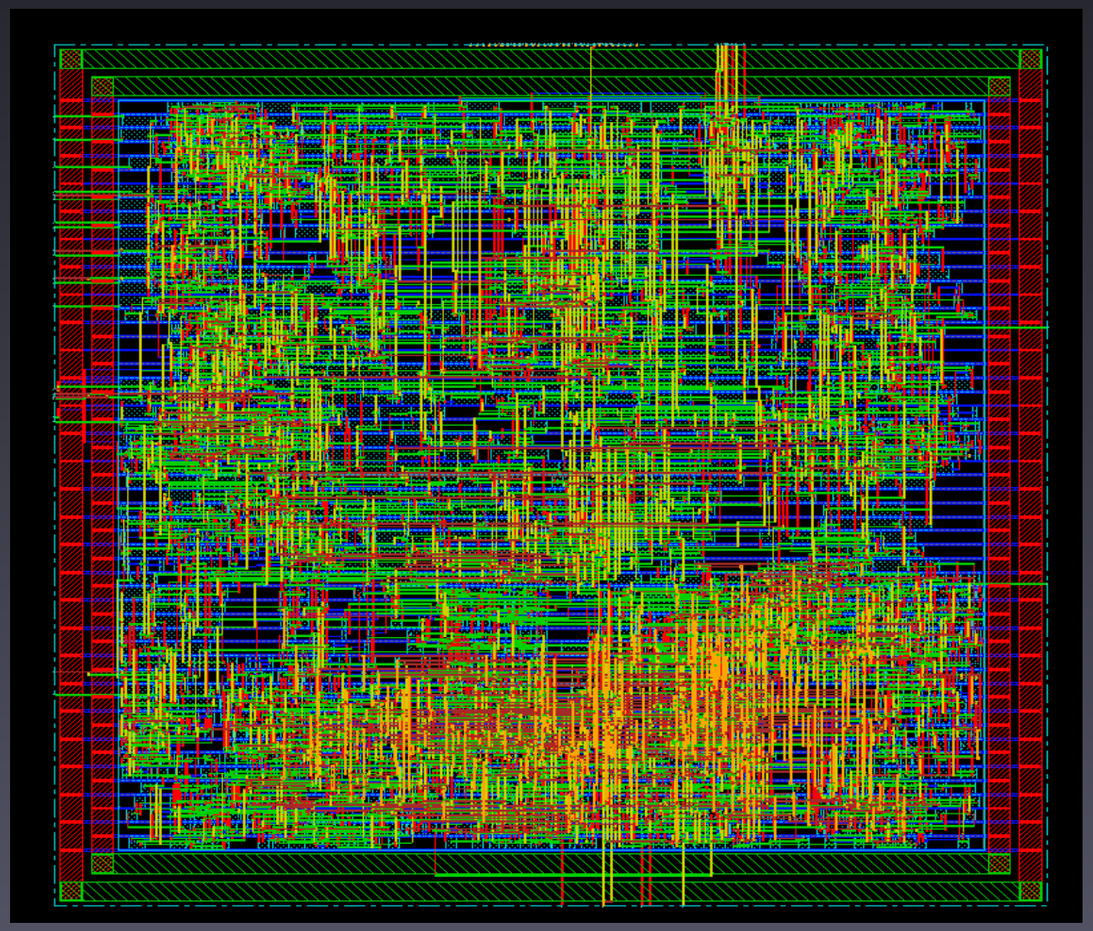
A Multi-Band RF Front End interface



A block of the video decoder

Microelectronics Group Research Topics

- SoC - Systems on a Chip
- NoC - Networks on Chip
- MEMs
- DSP Systems (video, voice, image)
- FPGA Design Methodologies



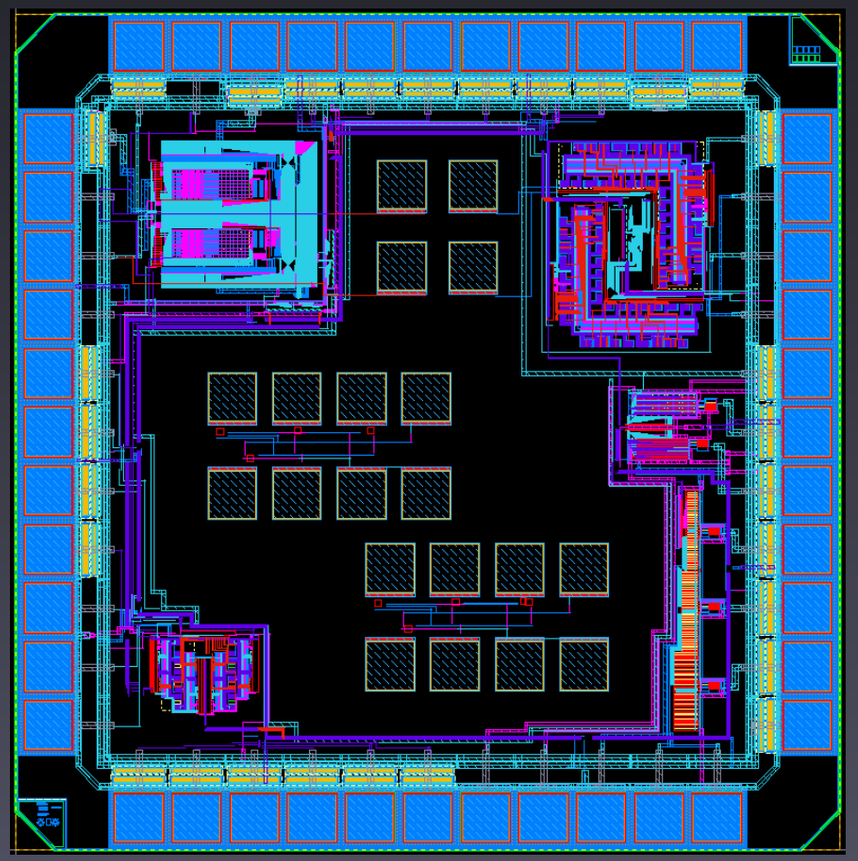
ASIC - CA-VL Coding module
CABAC coder/decoder - Parser

FPGA H.264 Coder prototyping

Microelectronics Group Research Topics

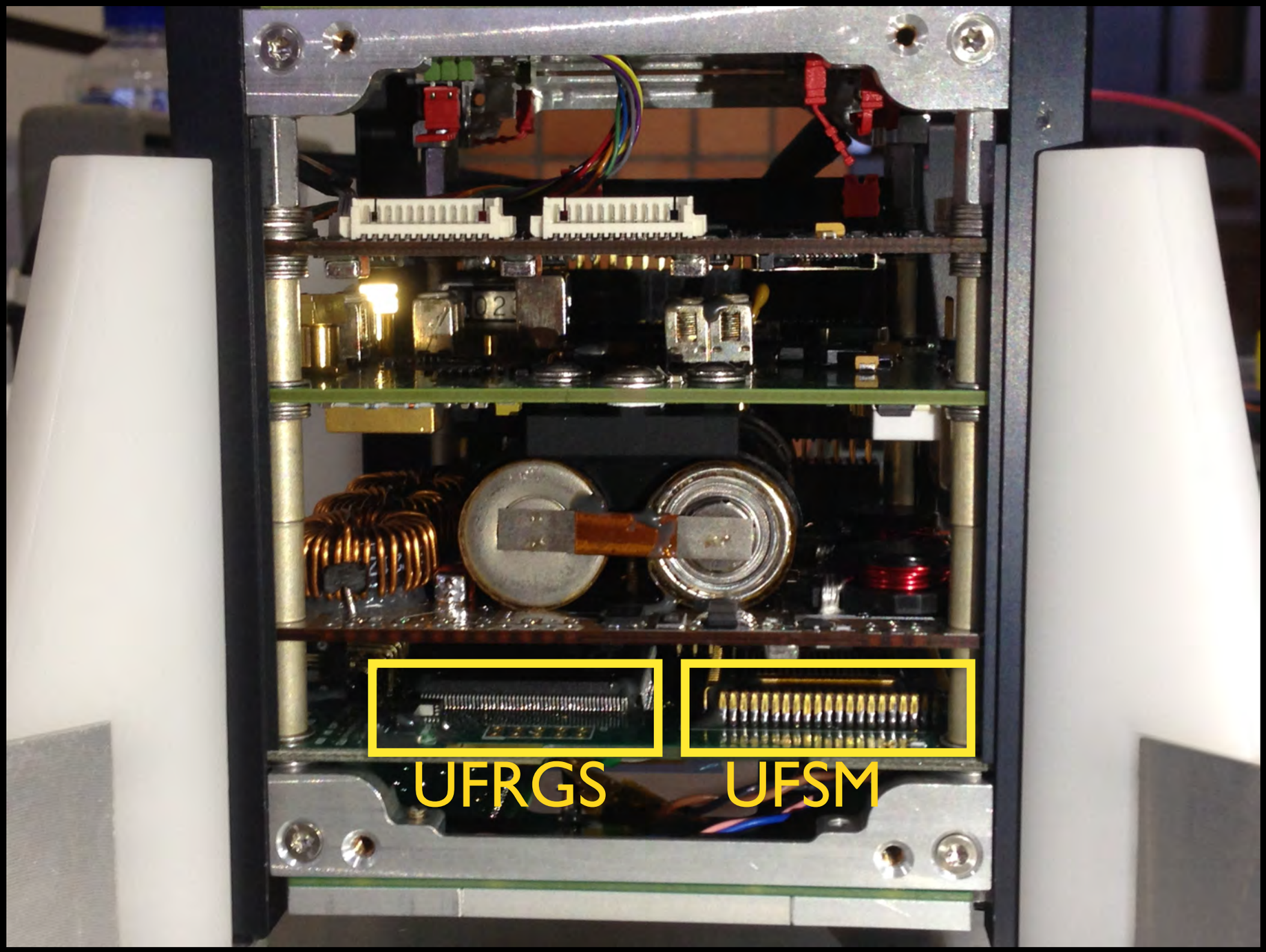
- Fault Tolerant Circuits
- Circuits Tolerant to Radiation Effects
- Variability
- Test
- Mixed Signal

Electrical testing of RFID 915MHz
(CEITEC Design)



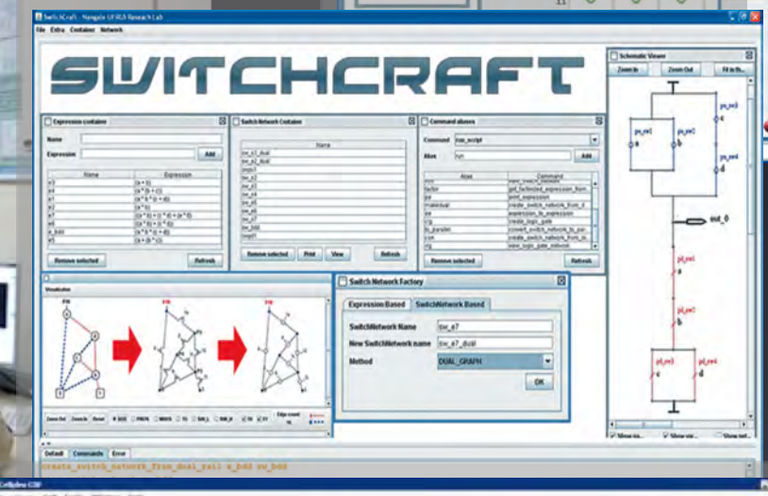
65nm CMOS Variability test structures

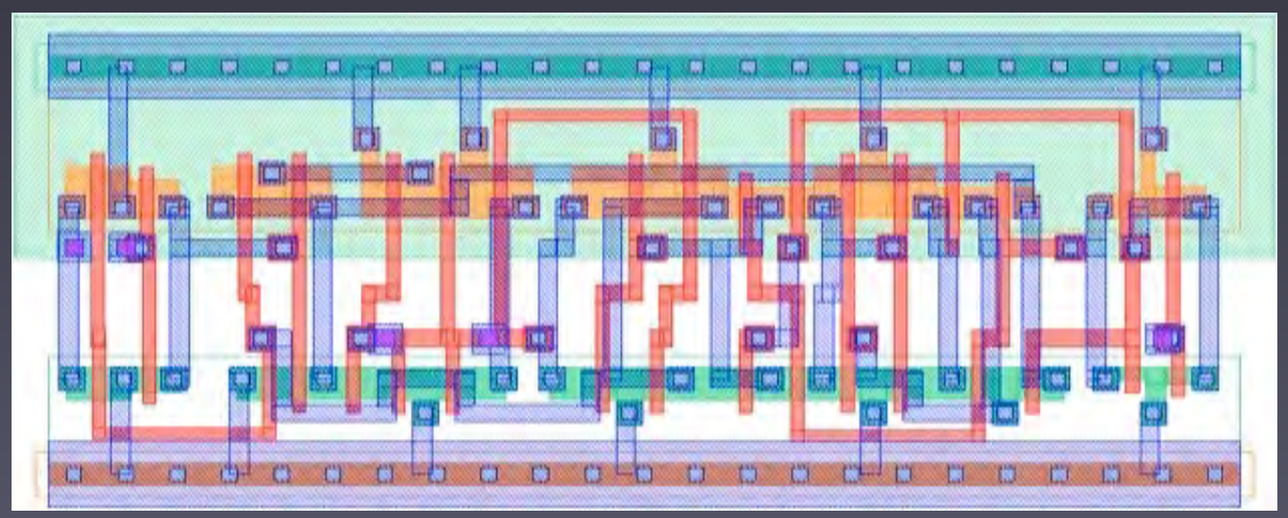
NanoSatC-BR1

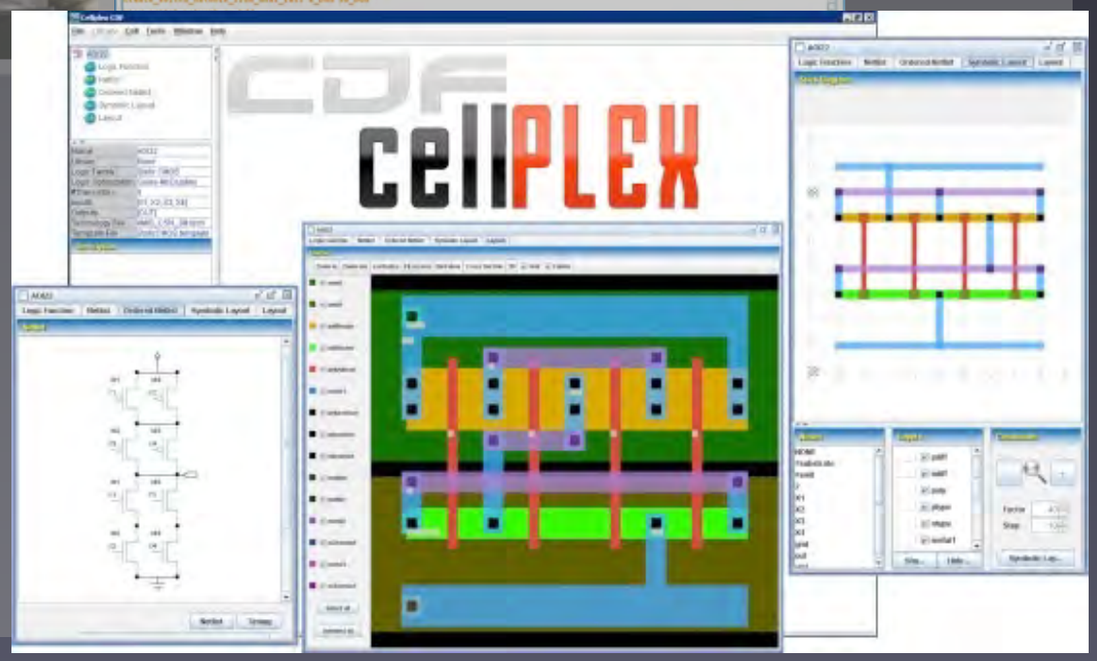


Microelectronics Group Research Topics

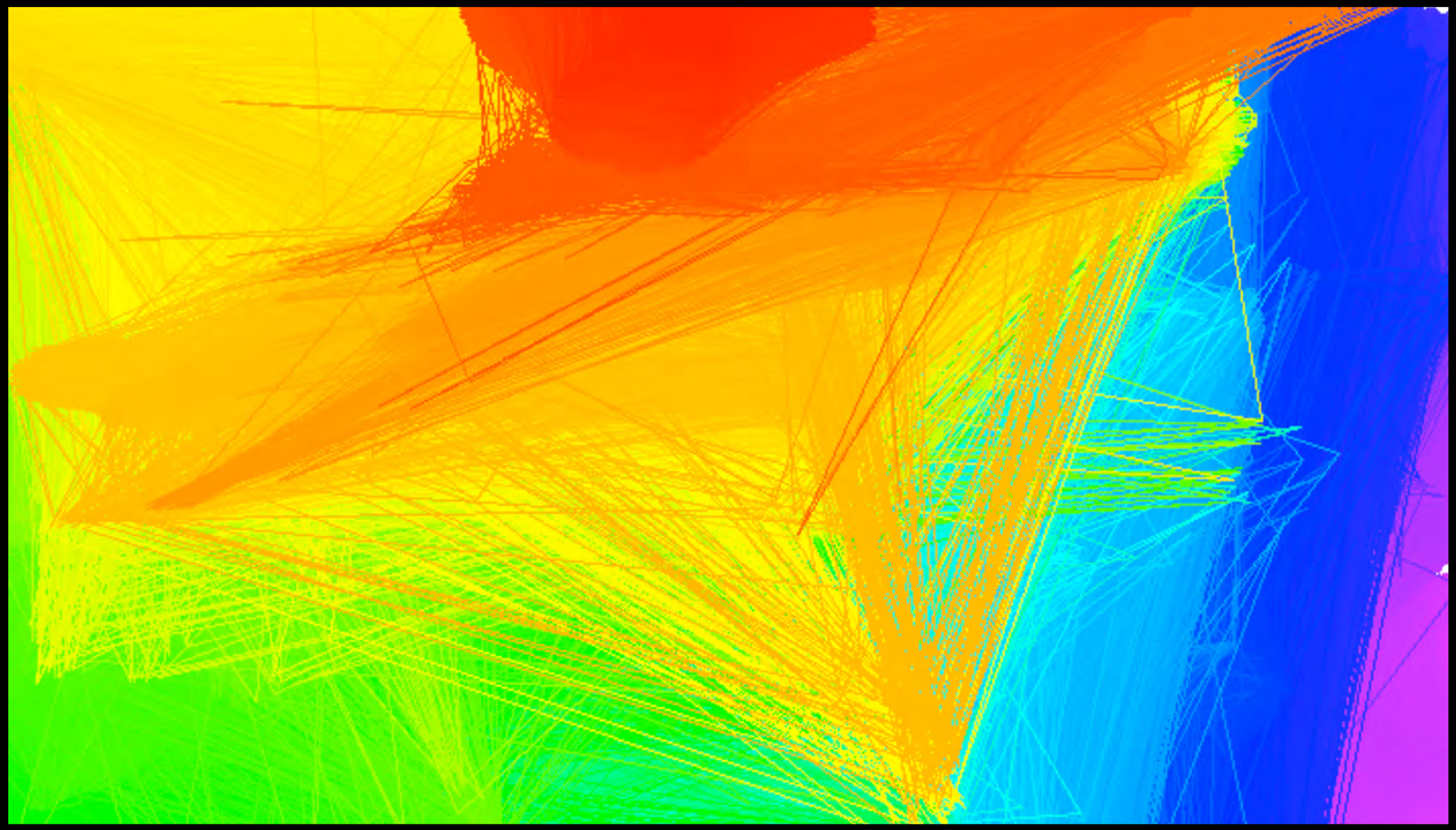
- Logic Synthesis
- Physical Design
- Design of Transistor Networks
- EDA Tools







Designed Automatically with ASTRAN



Visualization Tools

Ricardo Reis, Mateus Fogaça, Guilherme Flach

UFRGS

A bit of History

Visualization of Working Chips using E-Beam Microscope

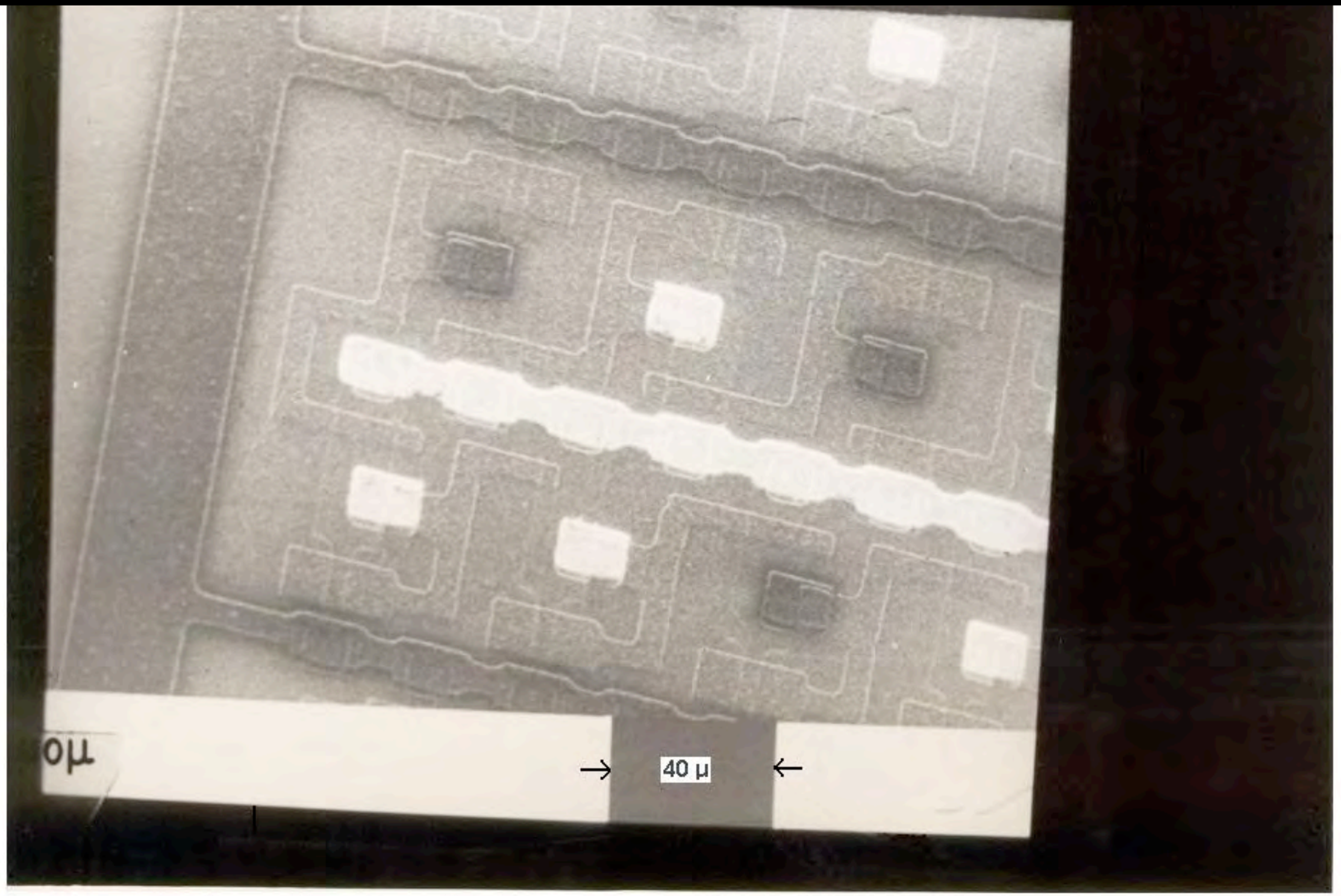
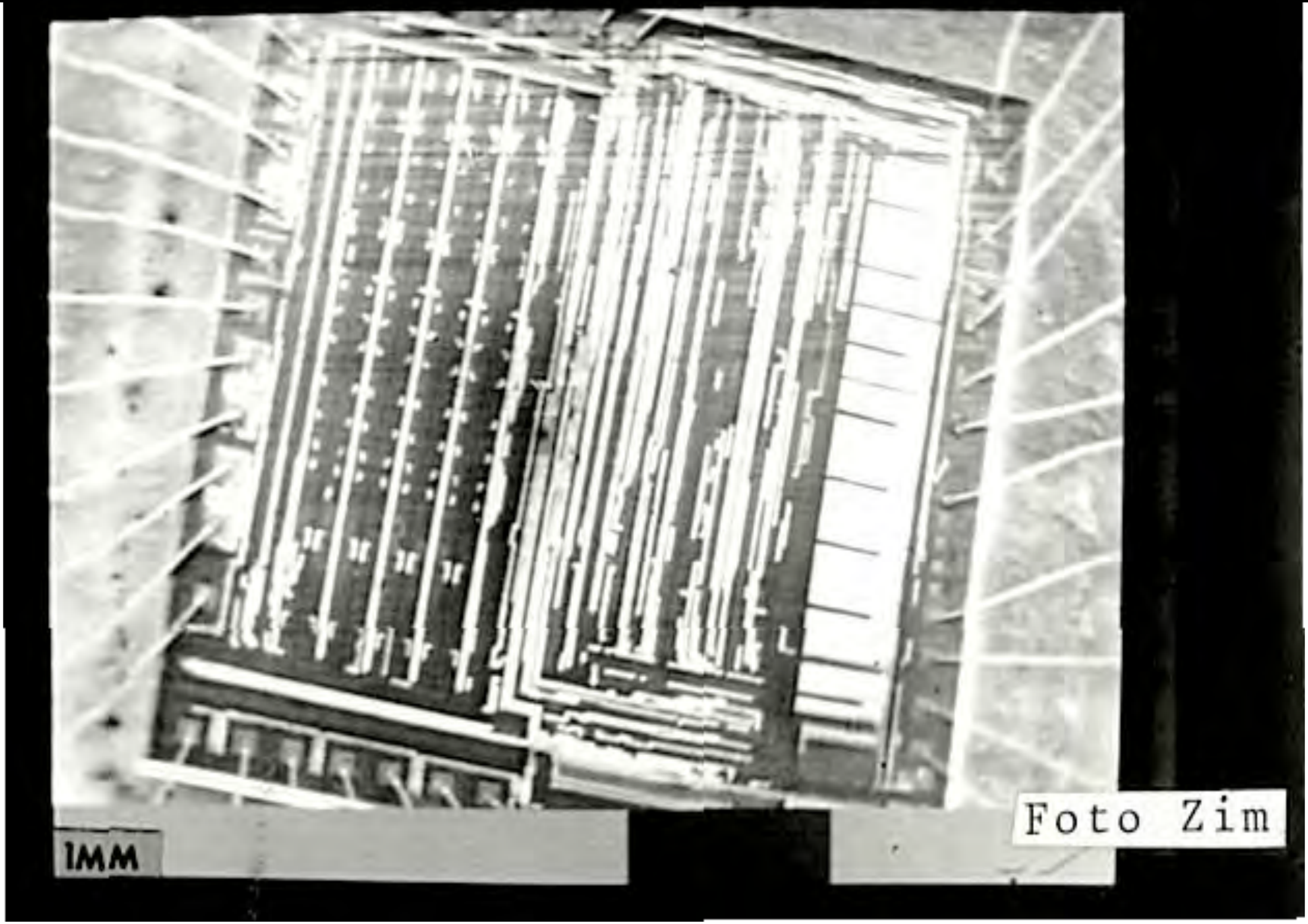


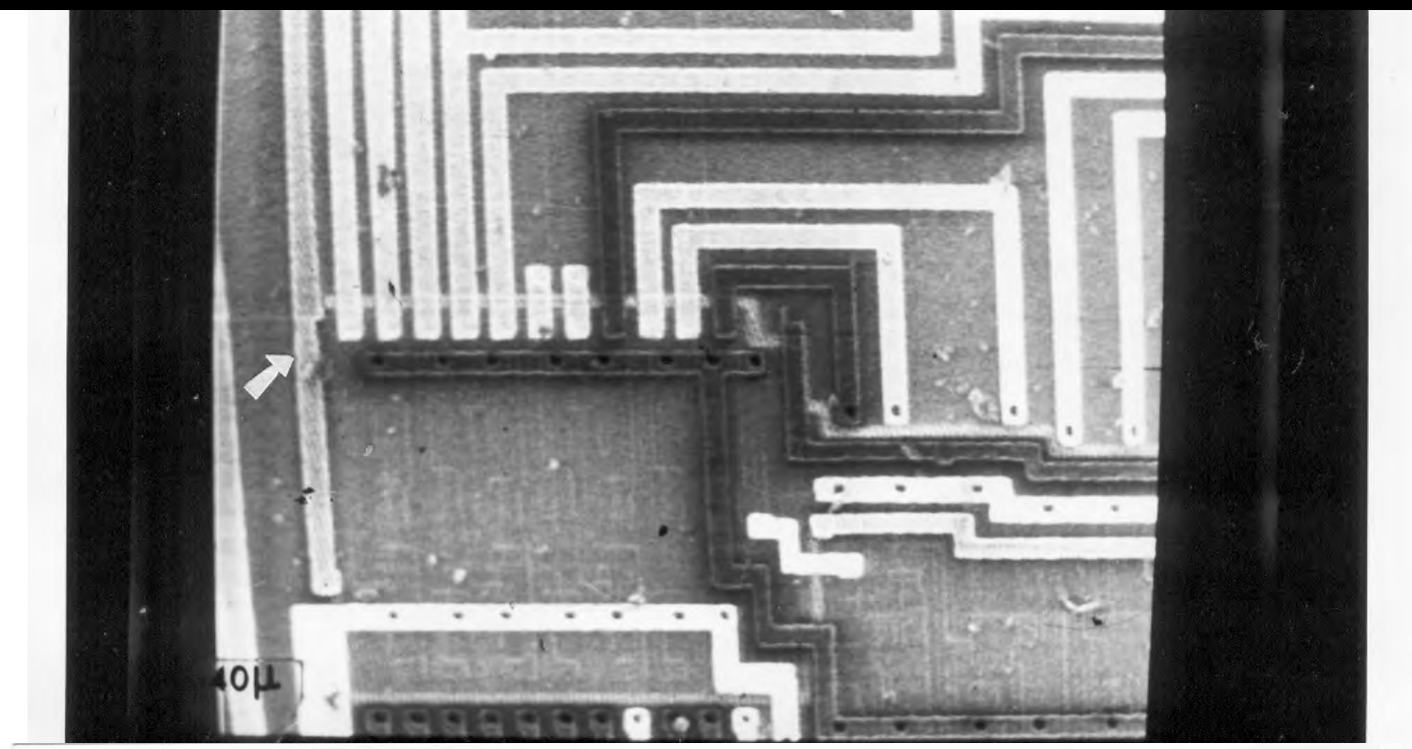
Image from Voltage Contrast (A= x500, E = 40 µm)

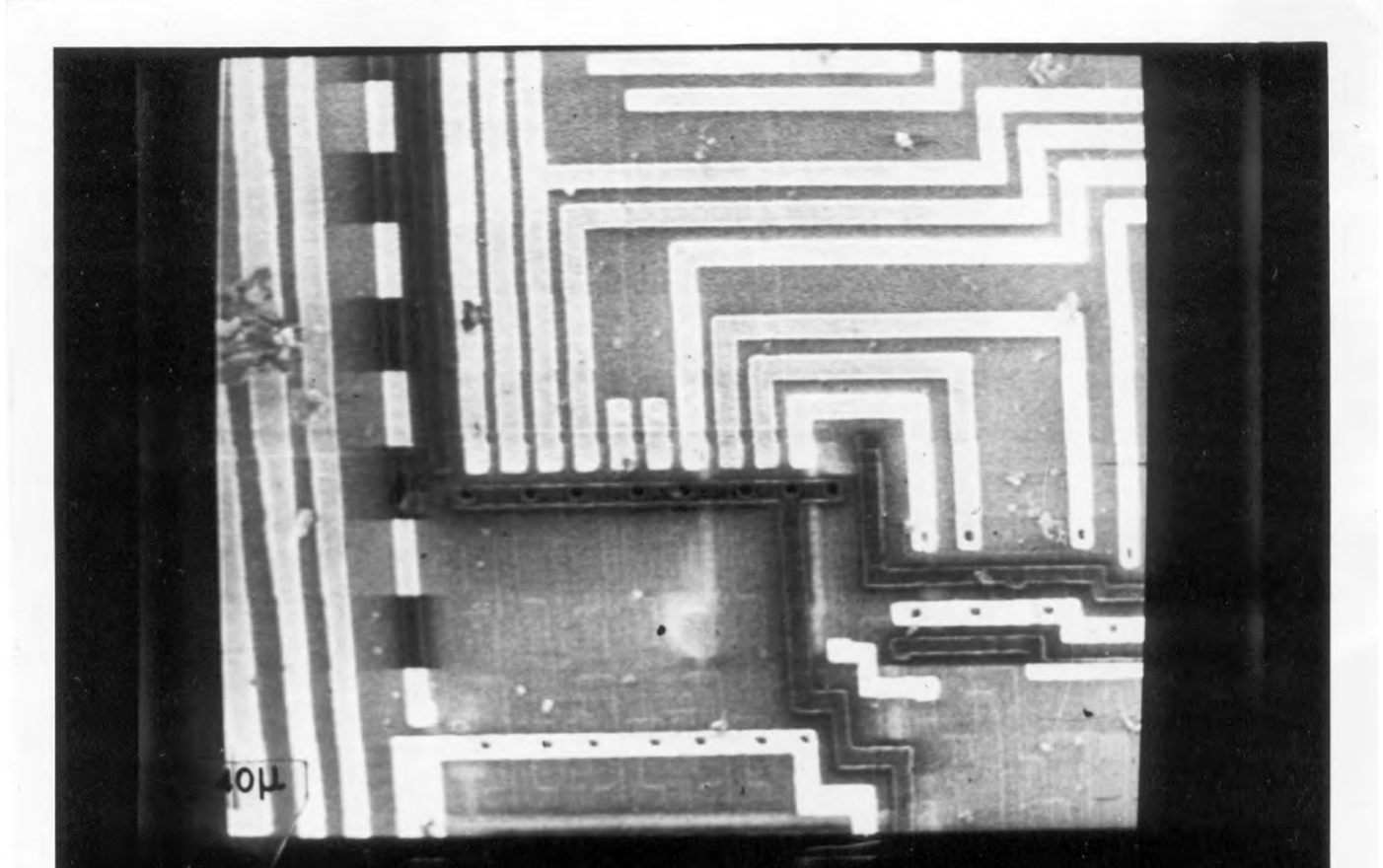
Carlos Hurtado UFRGS 1986

Visualization of Working Chips using E-Beam Microscope



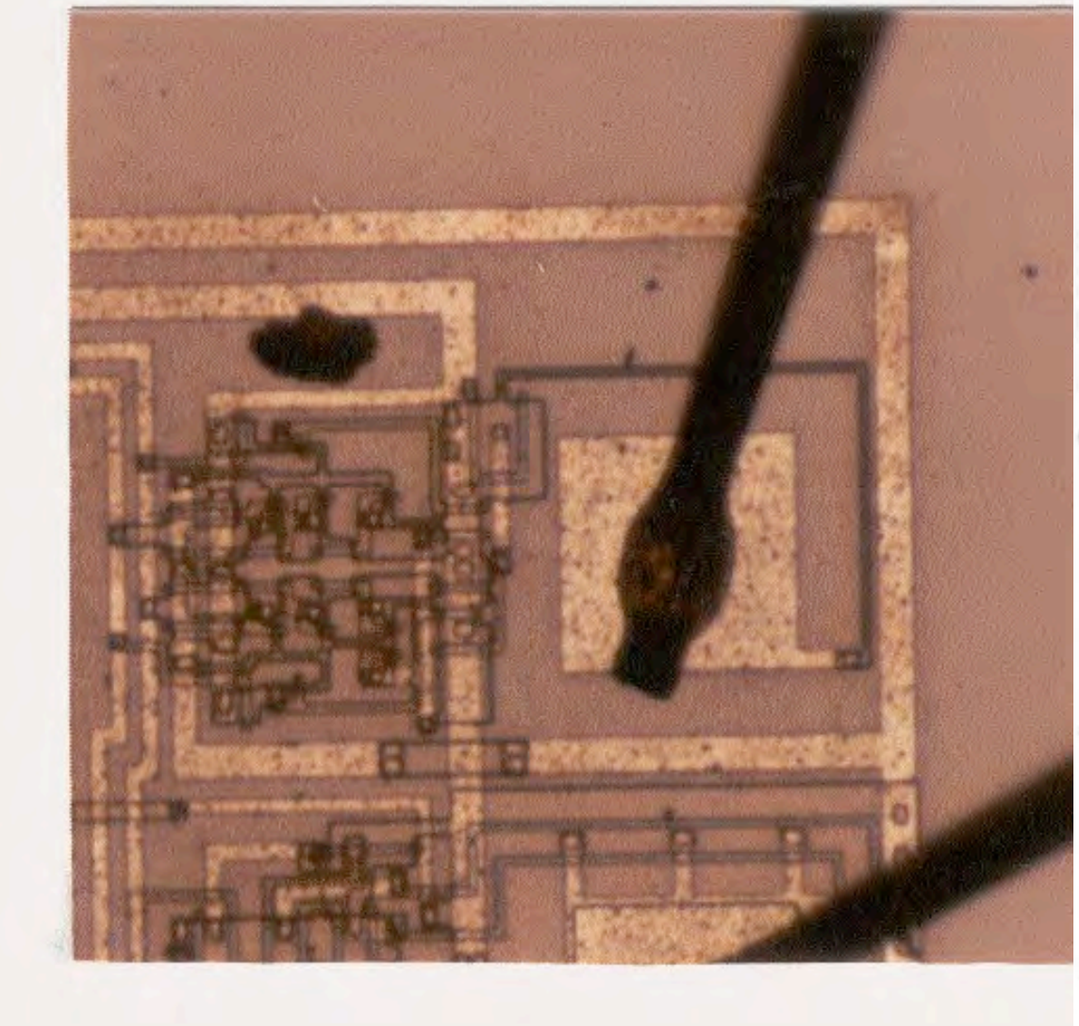
Visualization of Working Chips using E-Beam Microscope



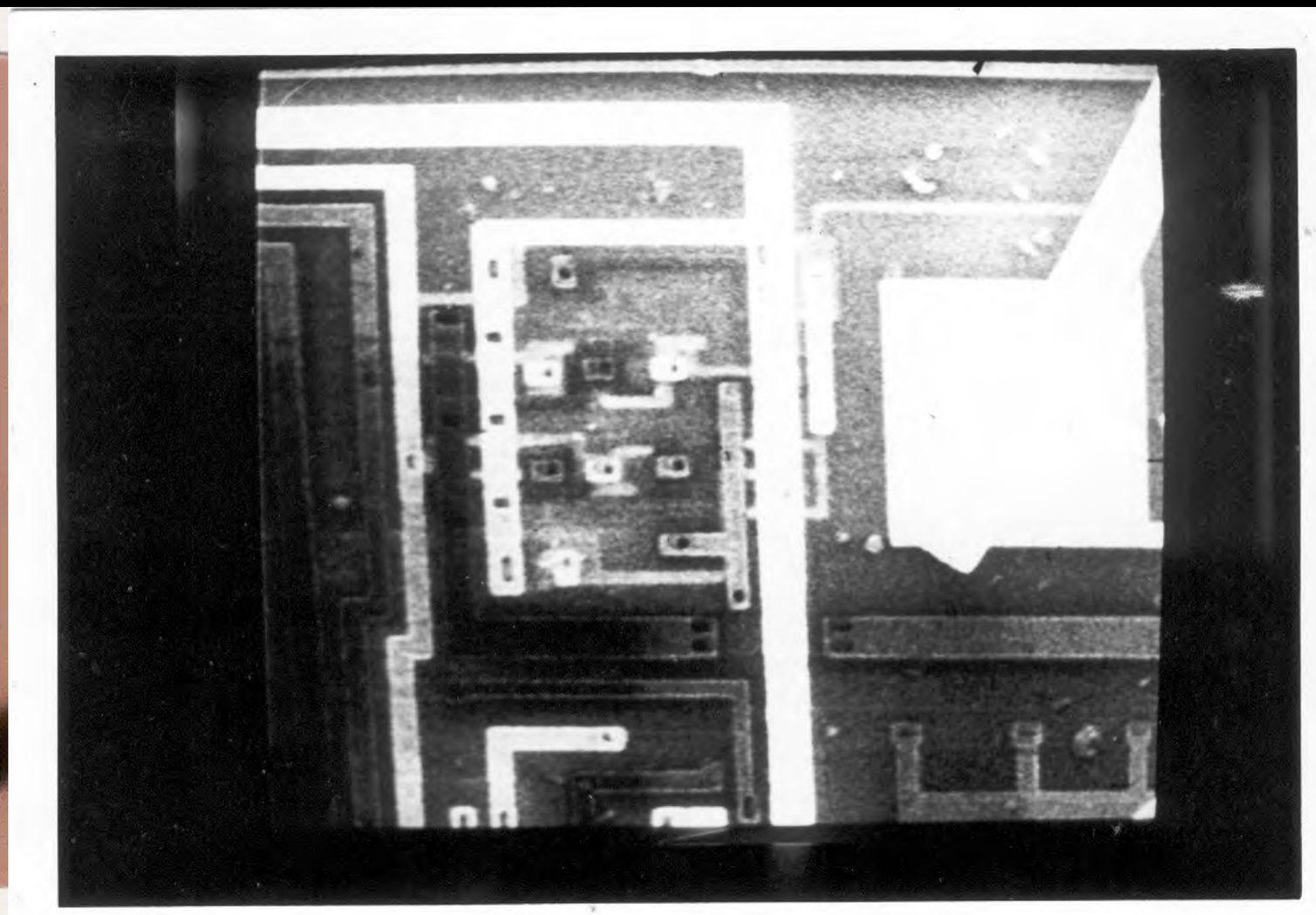


Observation of DC Signals (A= x500)
Carlos Hurtado 1986

Visualization of Working Chips using E-Beam Microscope



View of the Clock Pad with two phases
with an optical microscope (A= x200)



View of the Clock Pad at phase 1
with an EBeam microscope (A= x200)

Carlos Hurtado 1986

a new proposal…

A tool to emulate an E-Beam Microscope but using colors

one color for each layer

Dark color - zero

Light color - one

ex: dark blue - zero

light blue - one

Why Visualization Tools?

NanoCMOS design involves a **huge** amount of **information**!

Visualization tools associated to EDA tools helps to...

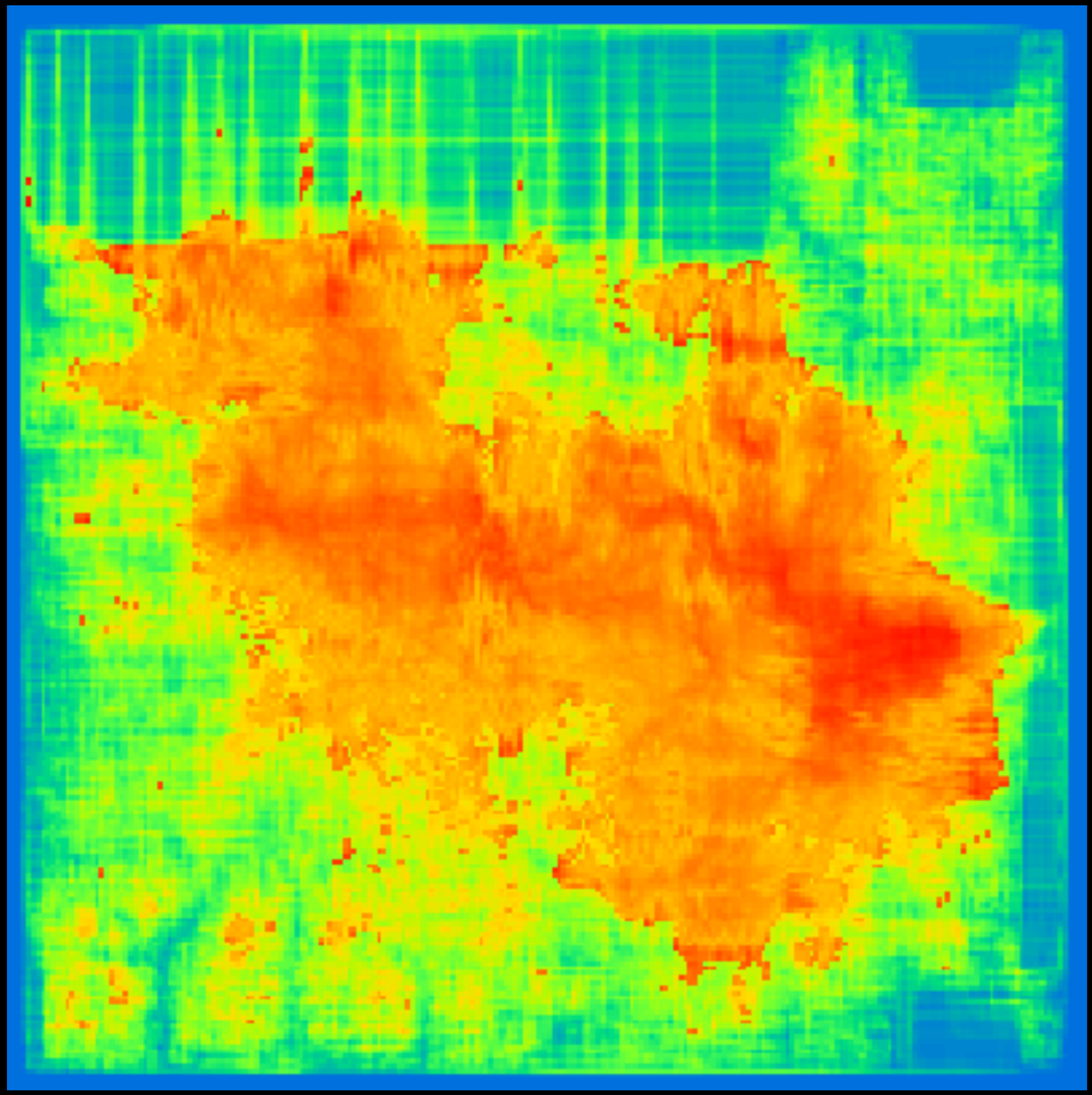
… **understand** an algorithm behaviour

… **evaluate** the quality of a solution

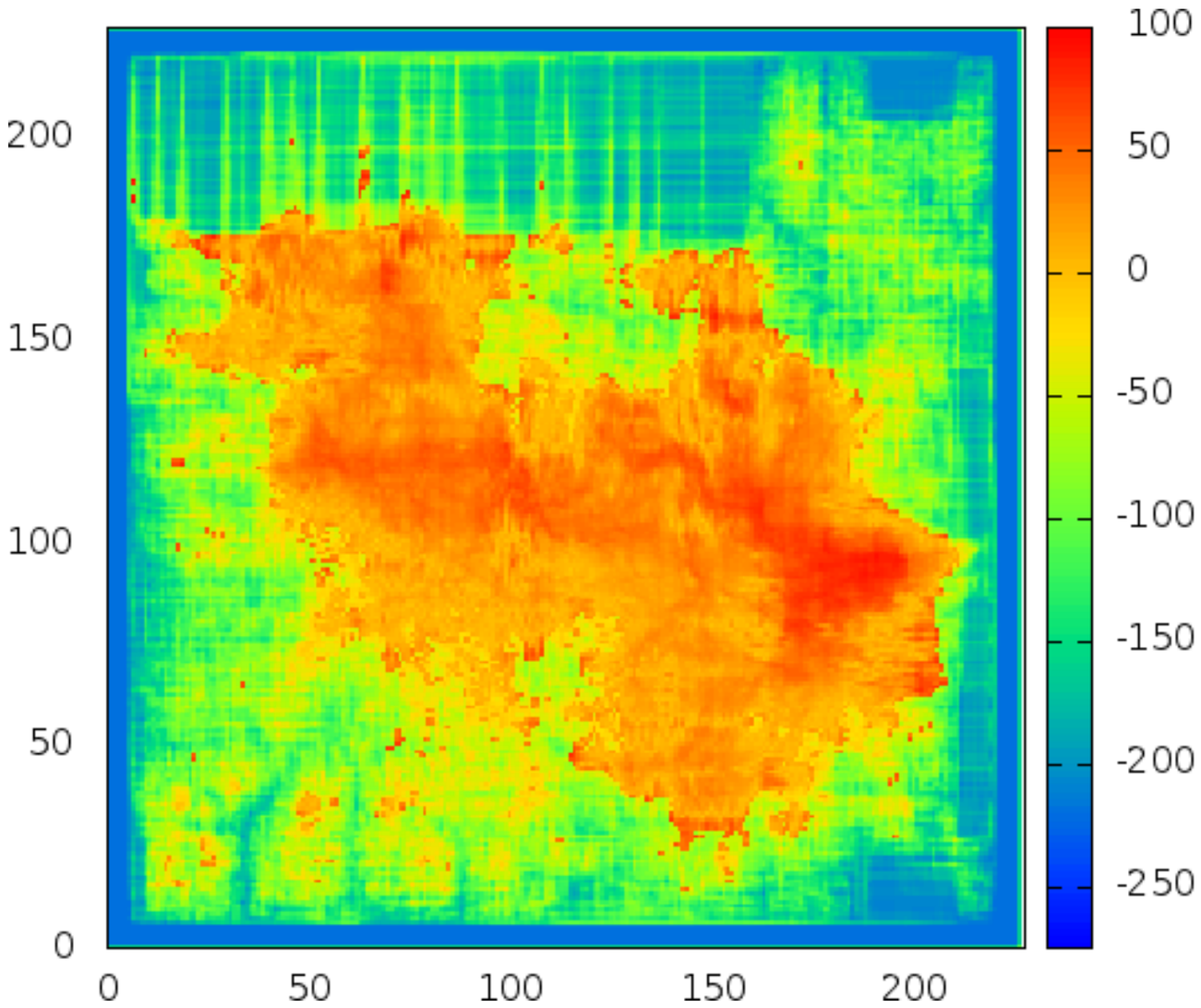
… design **debug**

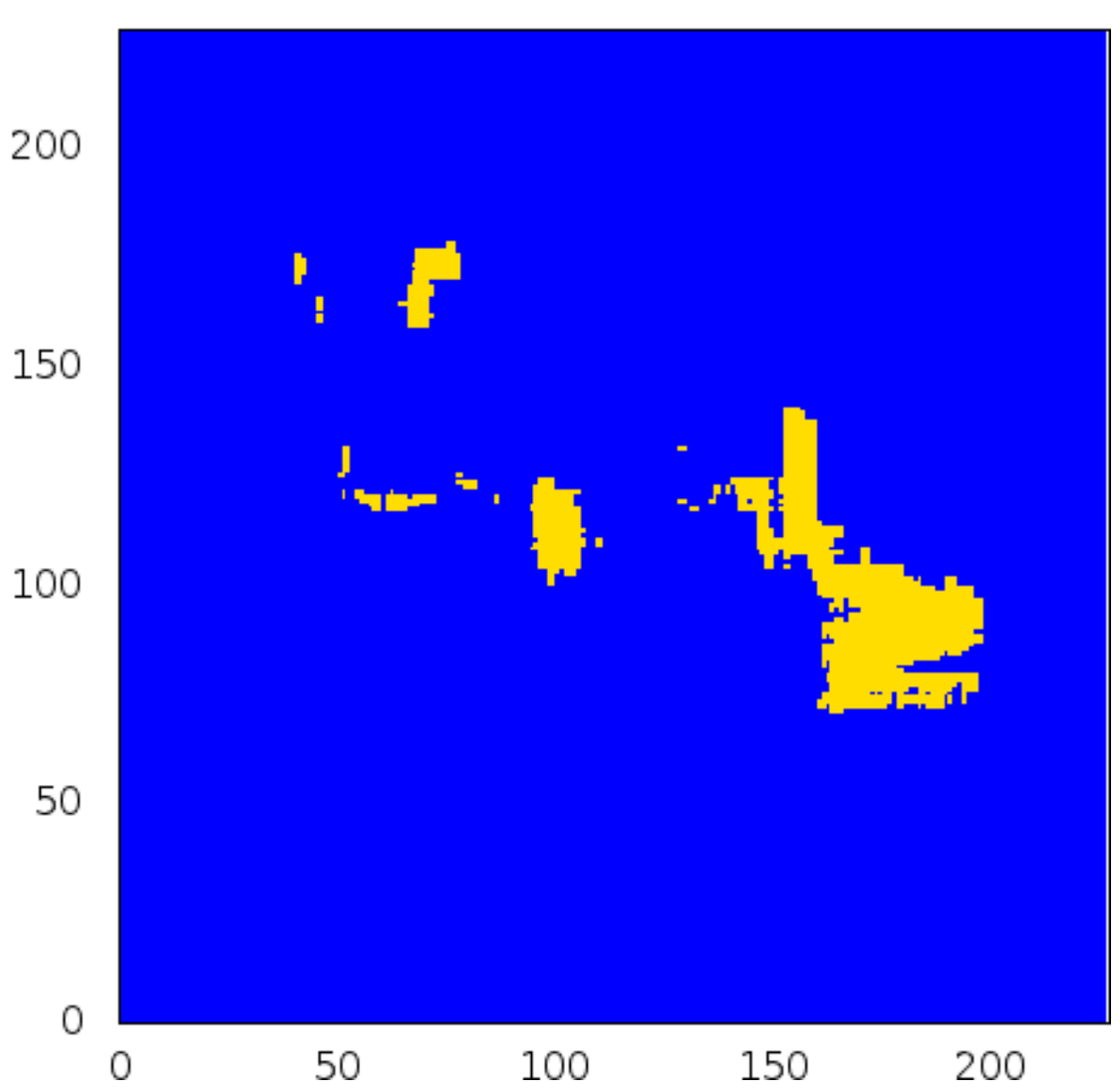
… design **improvement**

Hot Spot



Hot Spots Detection…





SET Simulation Results

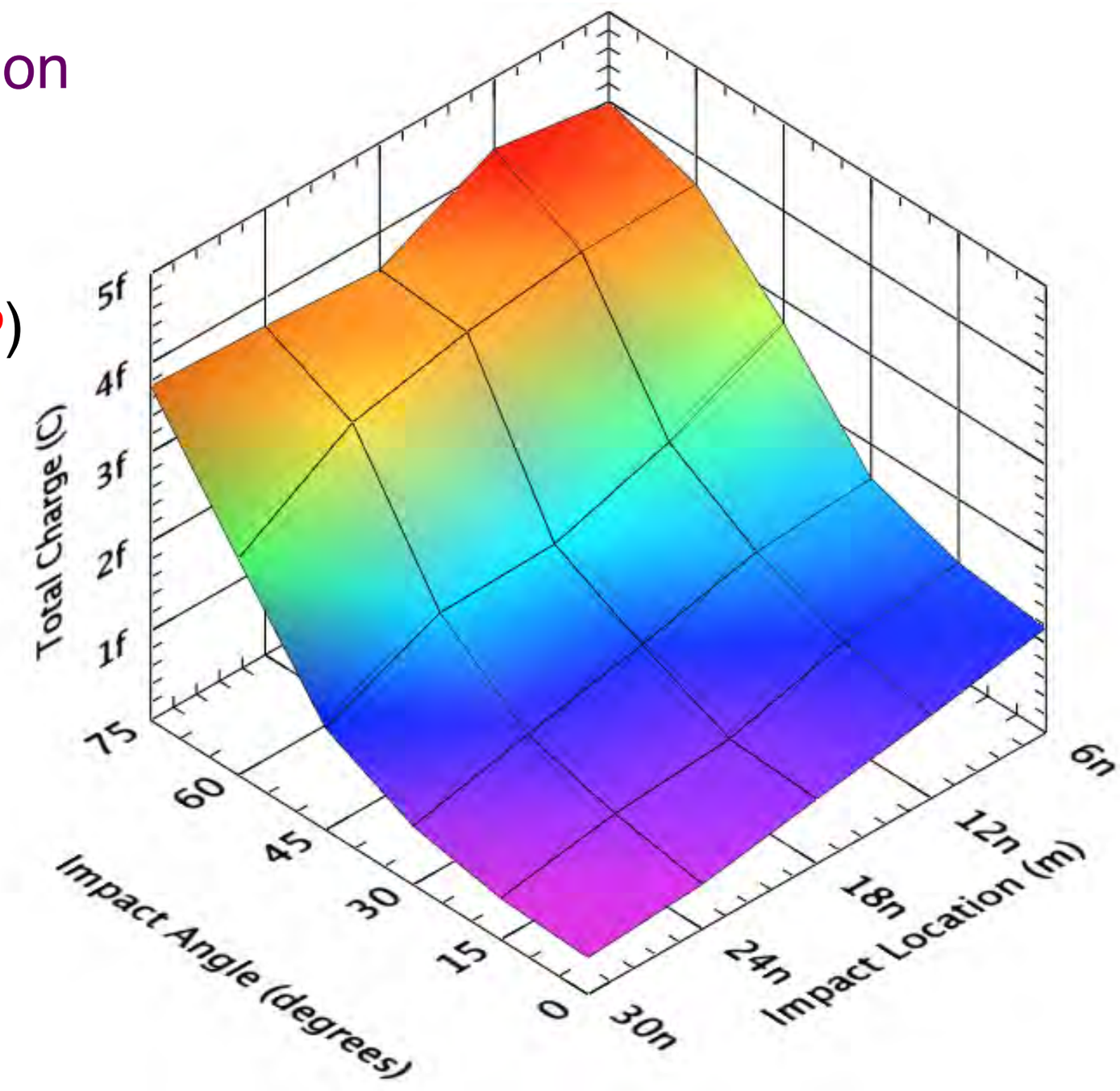
28nm FDSOI Drain Heavy Ion impact case:

CC_{max}= 4.20fC (L_i=12nm, θ=75°)

CC_{min}= 0.41fC (L_i=30nm, θ=0°)

When L_i ⬆ ➡ CC ⬇ .

When θ ⬆ ➡ CC ⬆ .

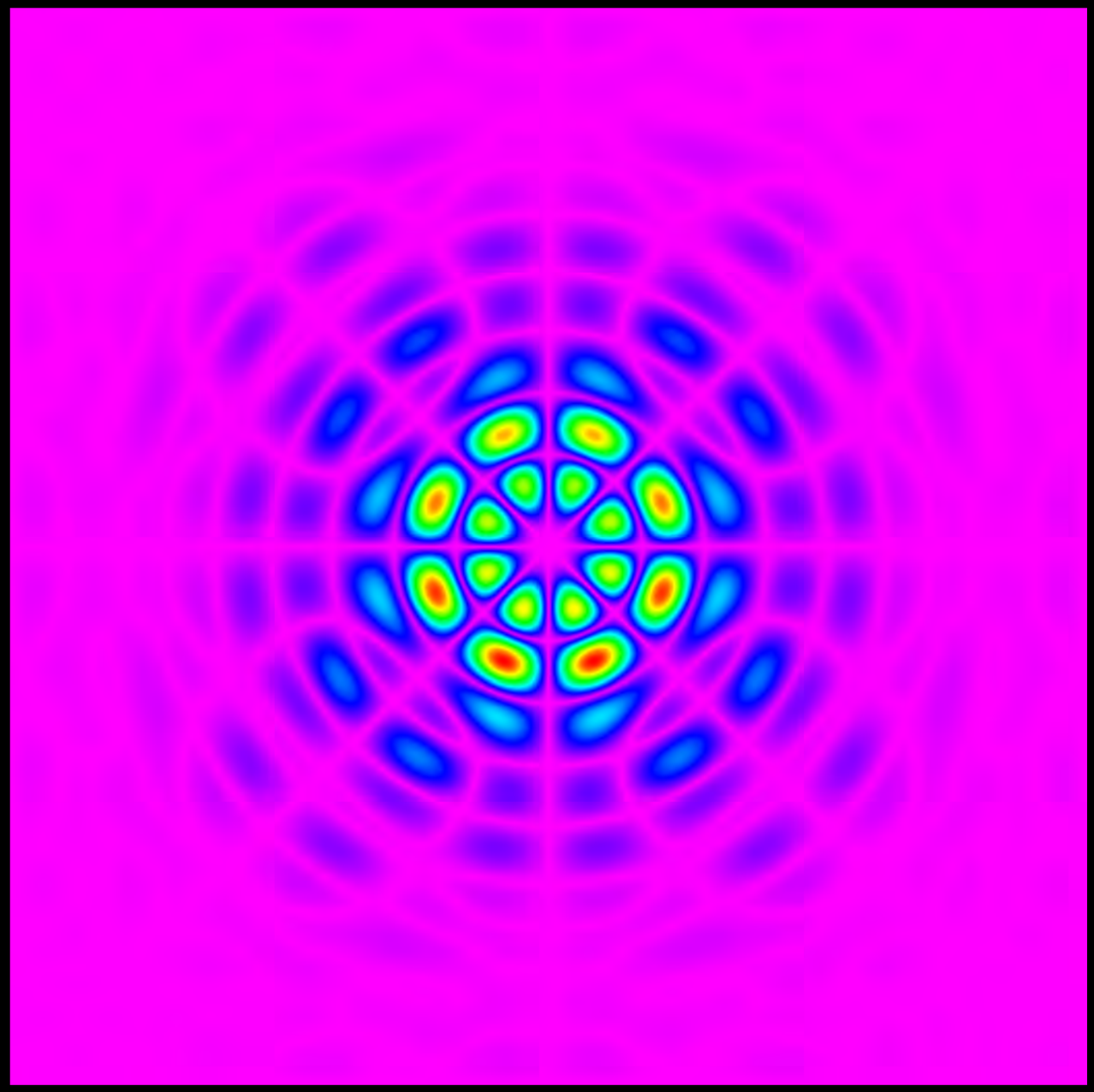


by Walter Bartra

A Tool to Simulate

Optical Lithography

in NanoCMOs



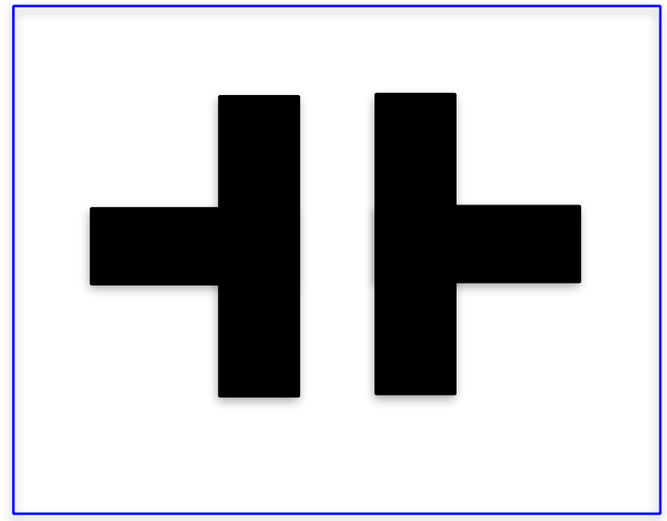
Tania Mara Ferla, Guilherme Flach, Ricardo Reis

OBS: This and other pictures will be presented at the DAC ART SHOW, Austin, Texas, June 6-9, 2016

A Problem in NanoCMOs

Why optical lithography is an issue?

Lost of resolution in nanometric technologies.



Technology Scaling

NTUEE/Y.-W. Chang

… and the technology node is at 14nm

!

Lithography Systems Evolution did not followed the technology scaling

Diffraction Problem: Some solutions...

Improvements in optical lithography system

Example: reduction of the wavelength

RET (resolution enhancement techniques):

→ DPL / MPL (multiple and double patterning lithography)

→ RDR (Restricted Design Rules)

→ OPC (Optical Proximity Correction)

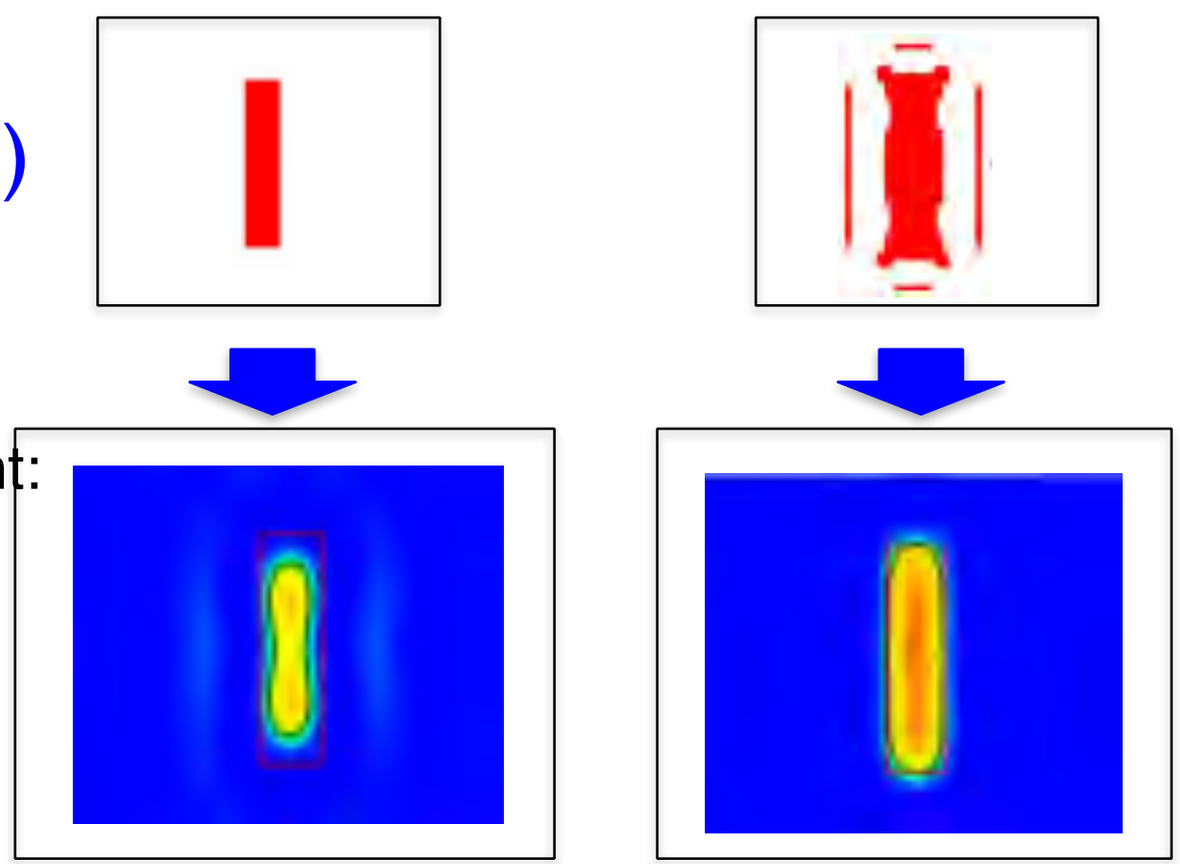
→ Regular Layout

Other Lithography Technologies under development:

Extreme Ultra-Violet Lithography (EUV)

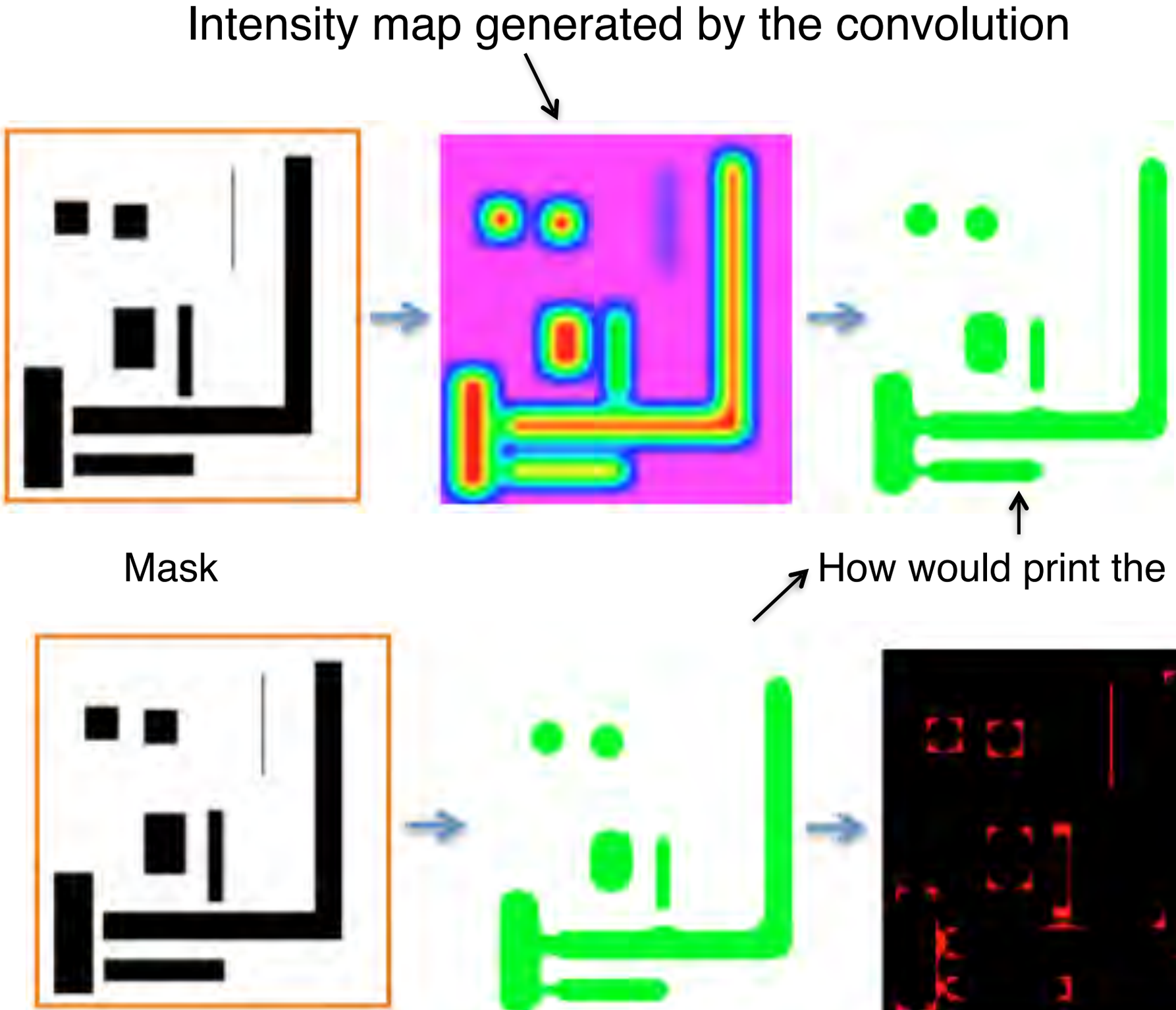
E-bream direct-write (EBDW)

Directed self-assembly (DSA)



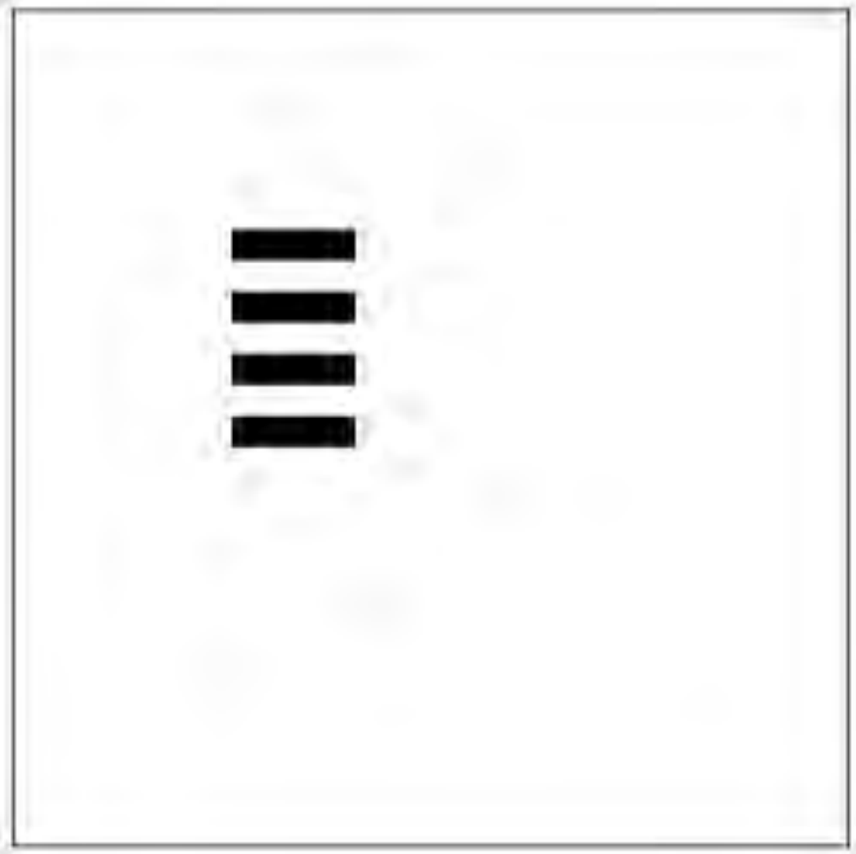
Li-Da Huang, 2004

Example of Simulation with the Tool

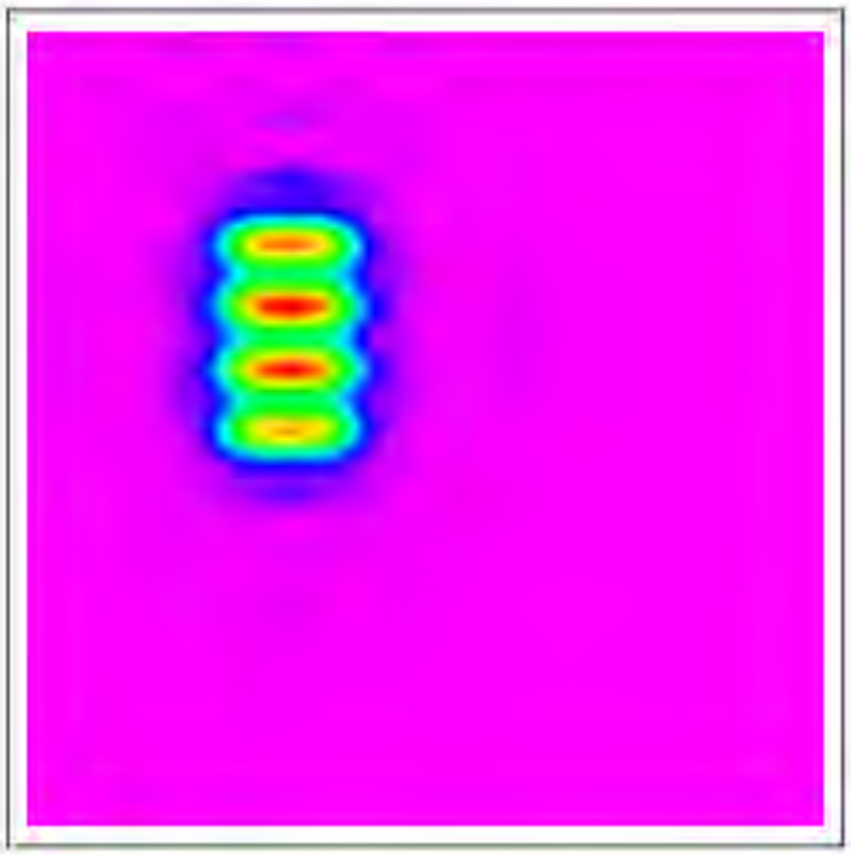


Lithux

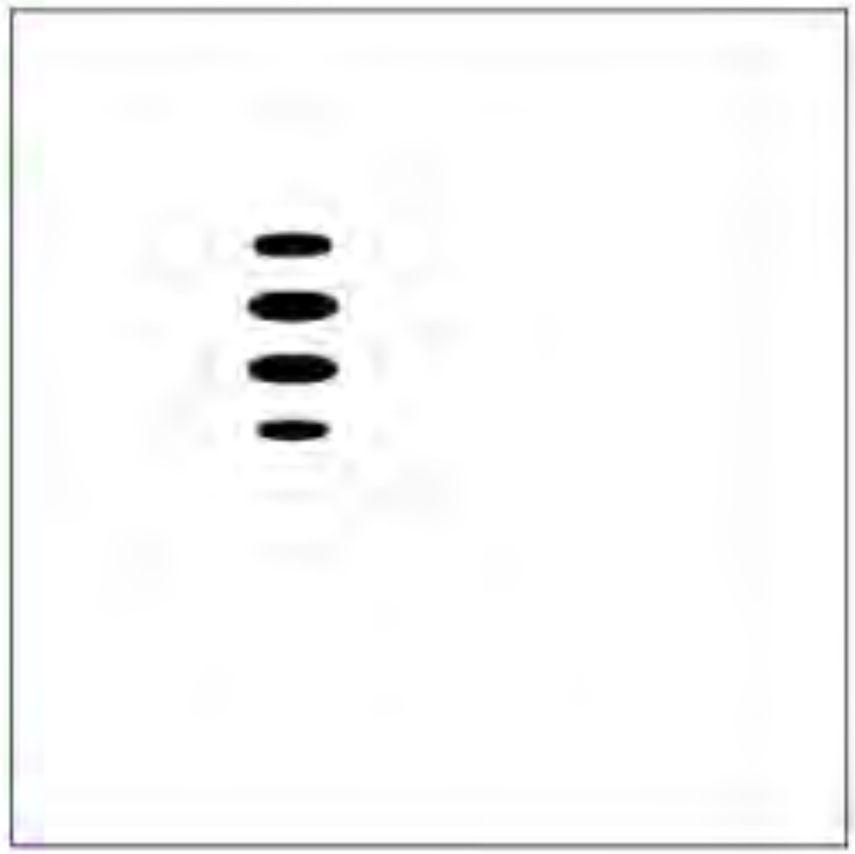
EDA tool for Lithography Simulation



Mask



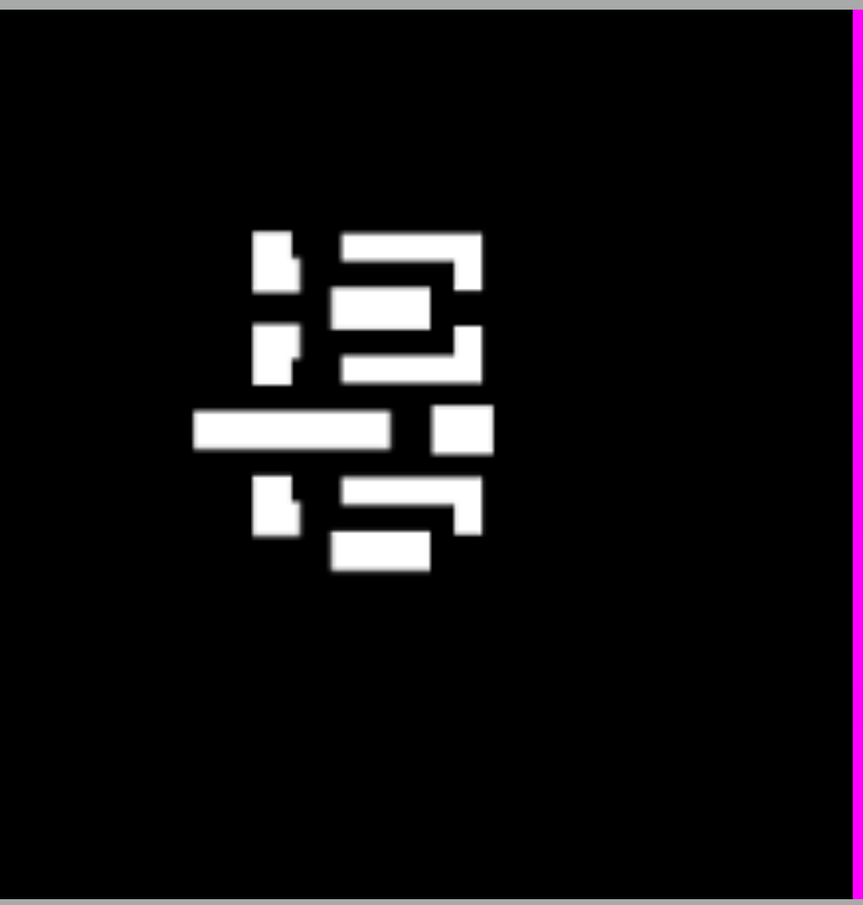
Intensity Map



Printing Pattern

Lithux

EDA tool for Lithography Simulation



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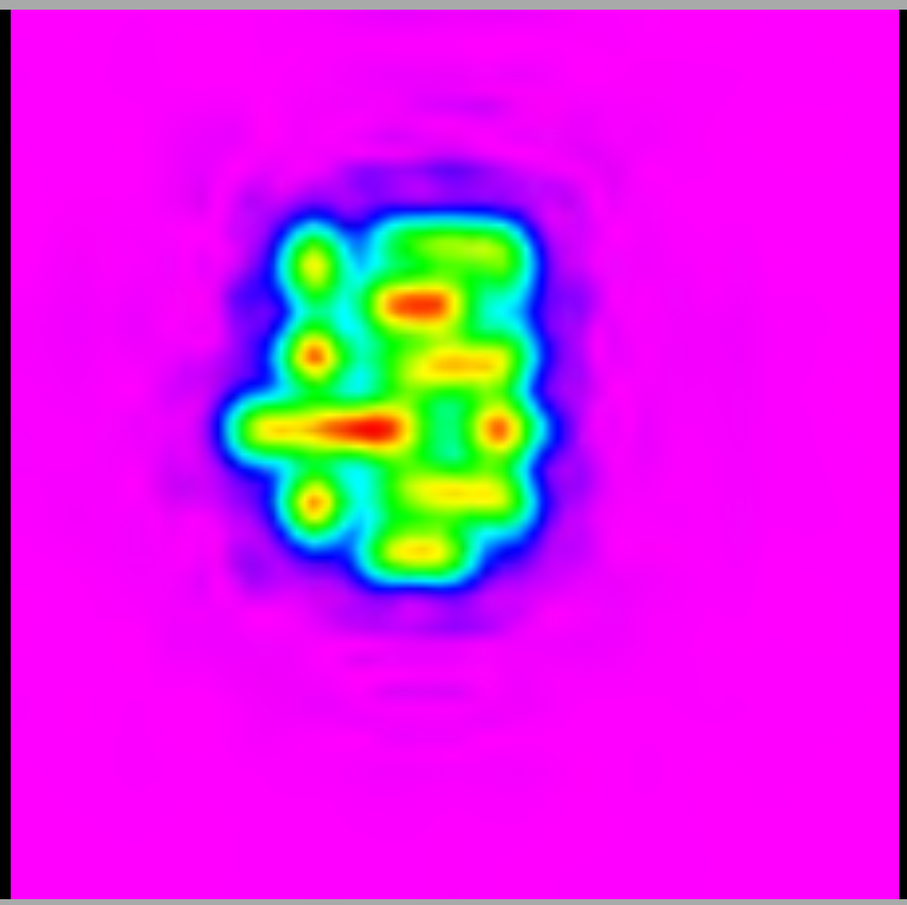
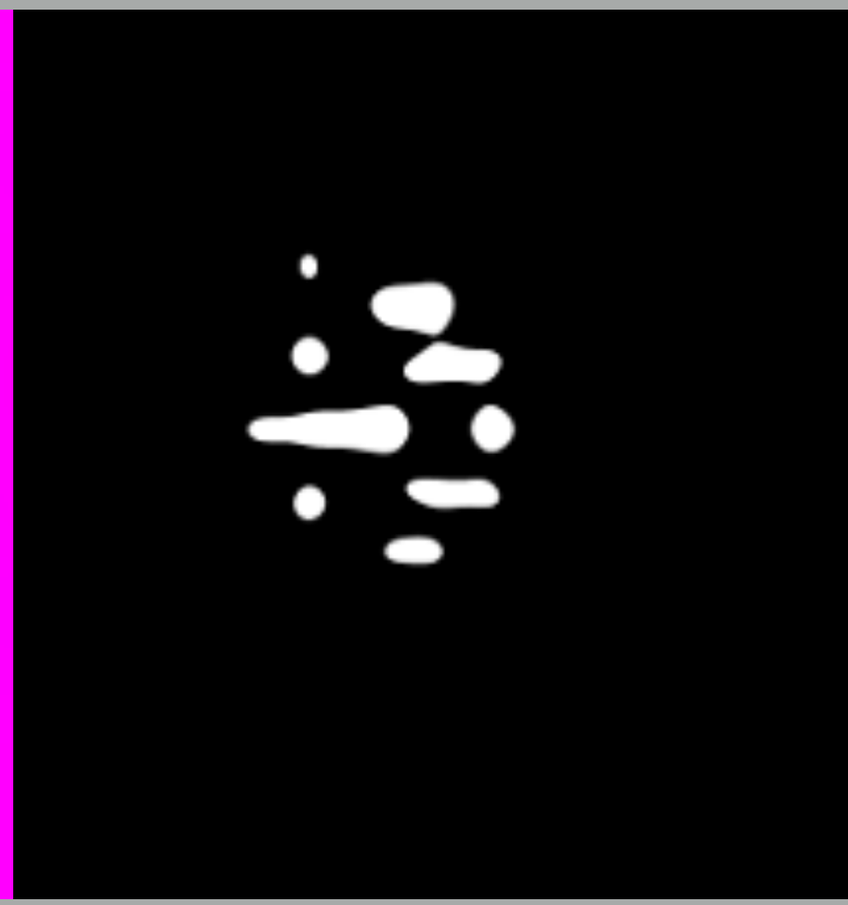


Intensity Map

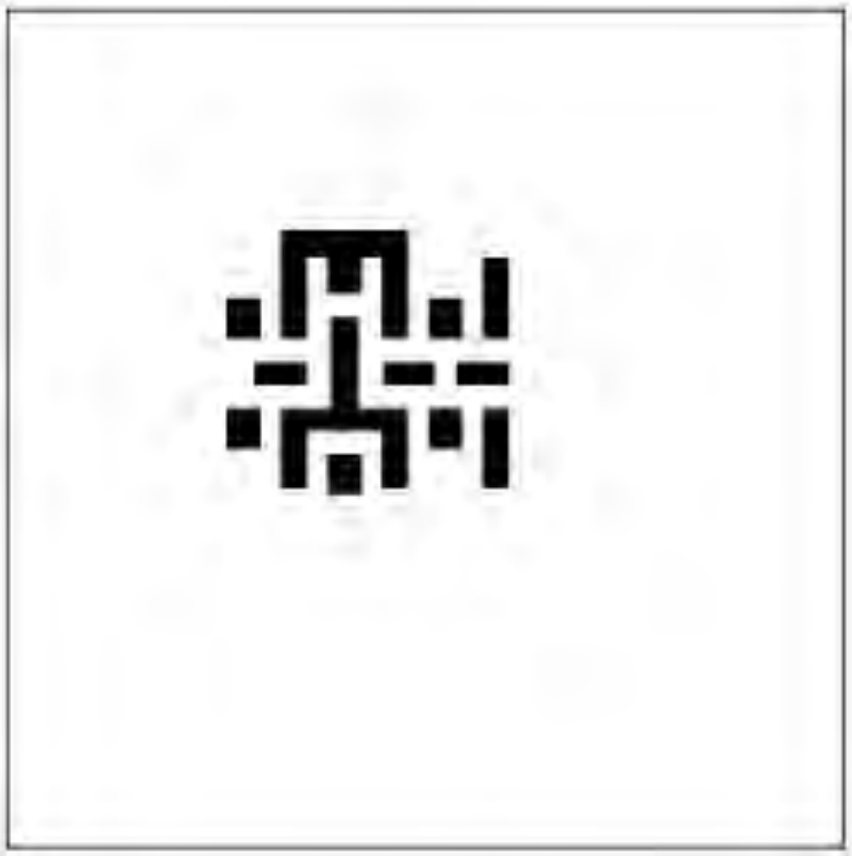


Printing Pattern

Tania Ferla

Lithux

EDA tool for Lithography Simulation



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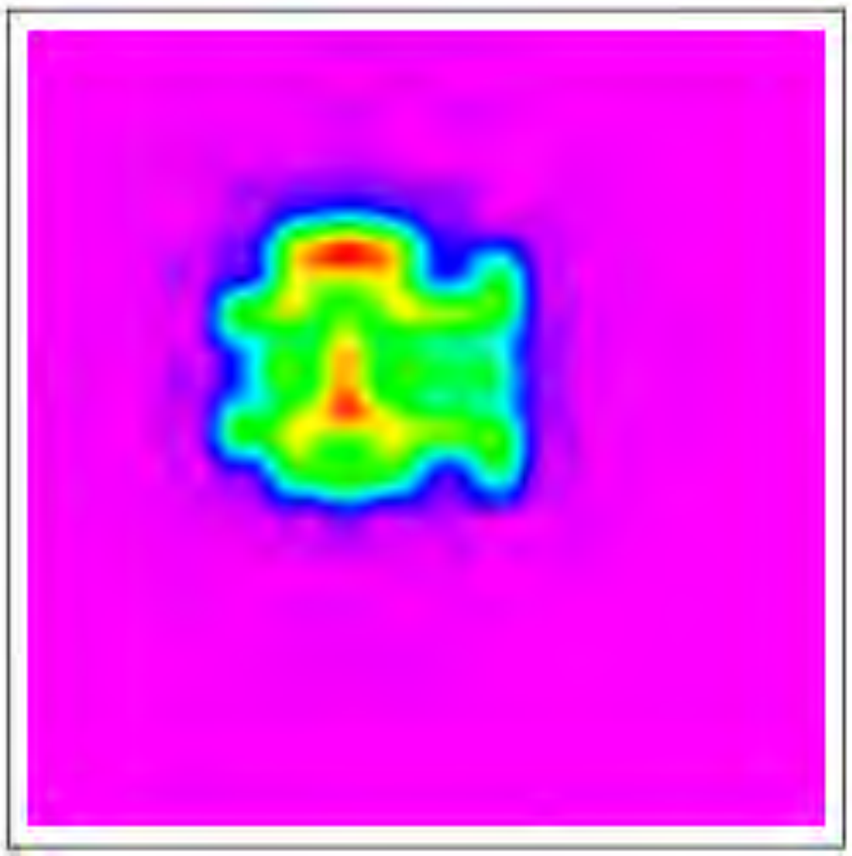
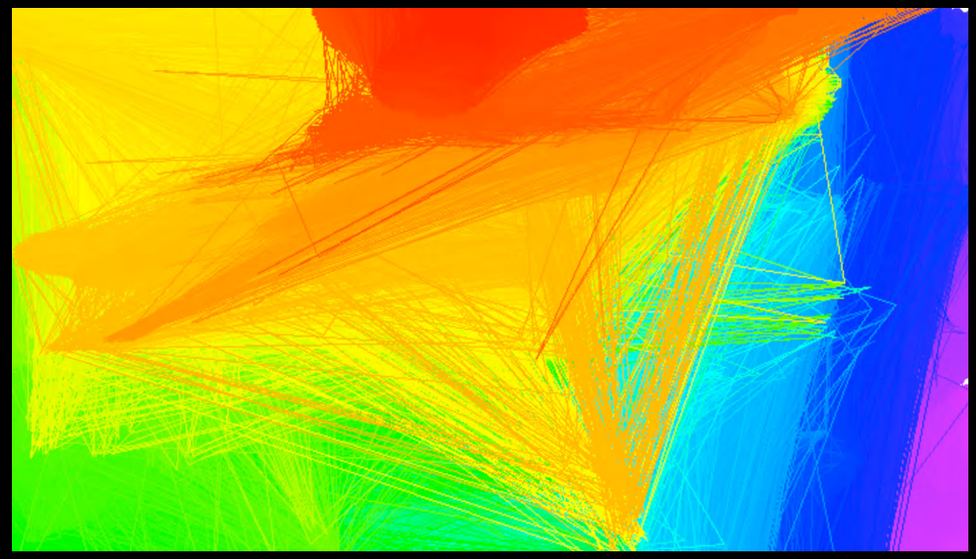


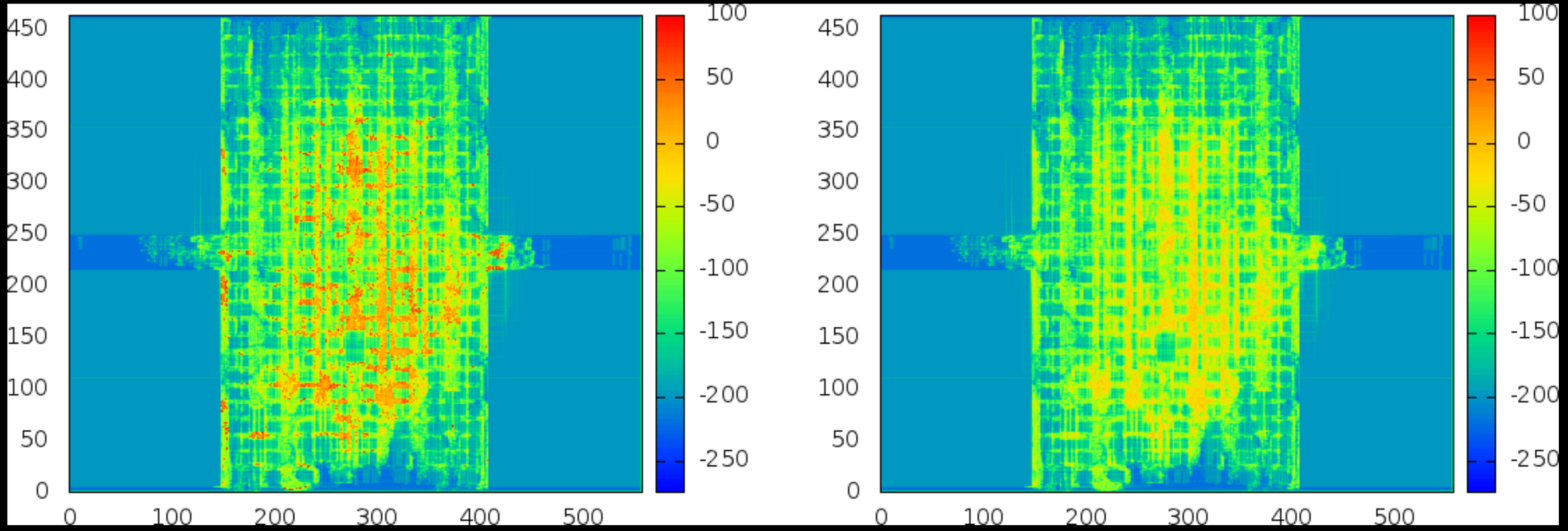
Intensity Map

Printing Pattern

Routing

Global Routing
Detailed Routing





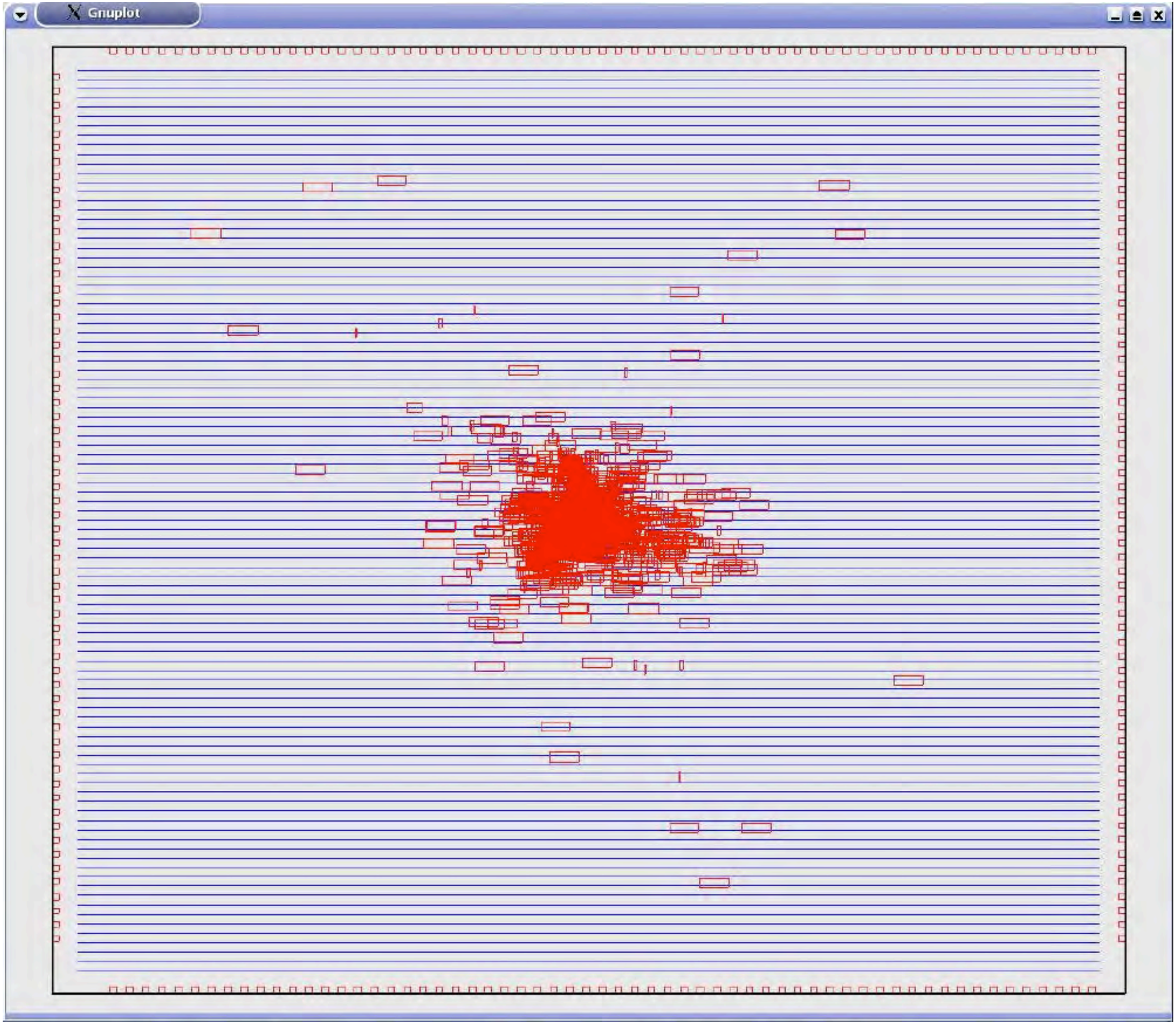
Congestion Map

Visualisation Tools

helping

Placement tools

improvement

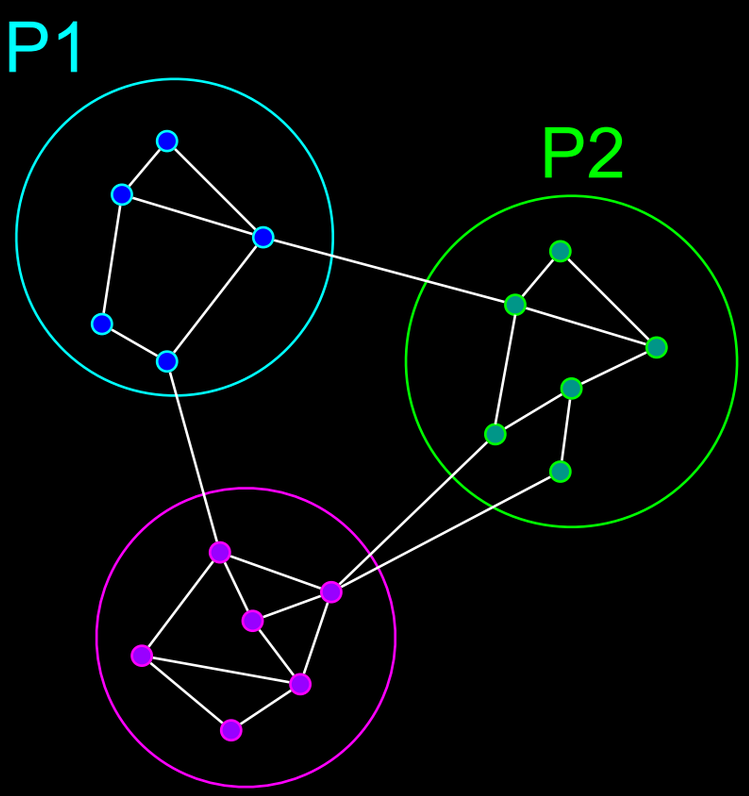

Gnuplot

Understanding an Algorithm Behaviour

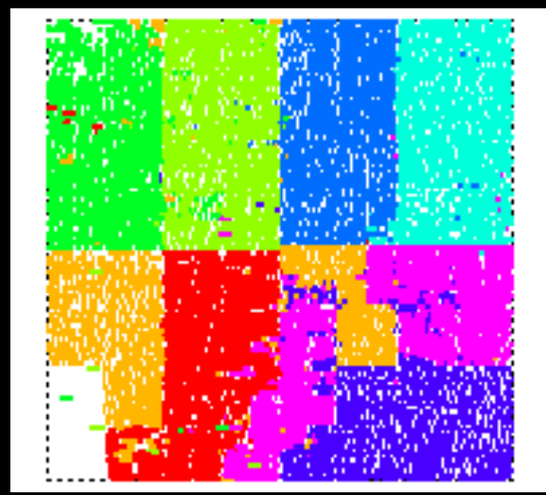
Placement Colouring[1]

Netlist

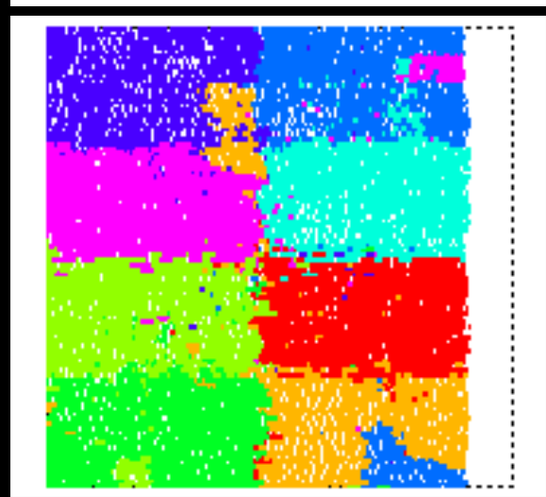
Graph partitioning tool



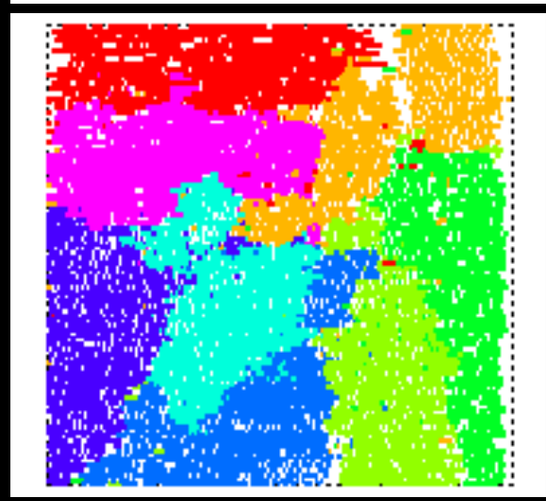
Placement coloring



Capo



Dragon

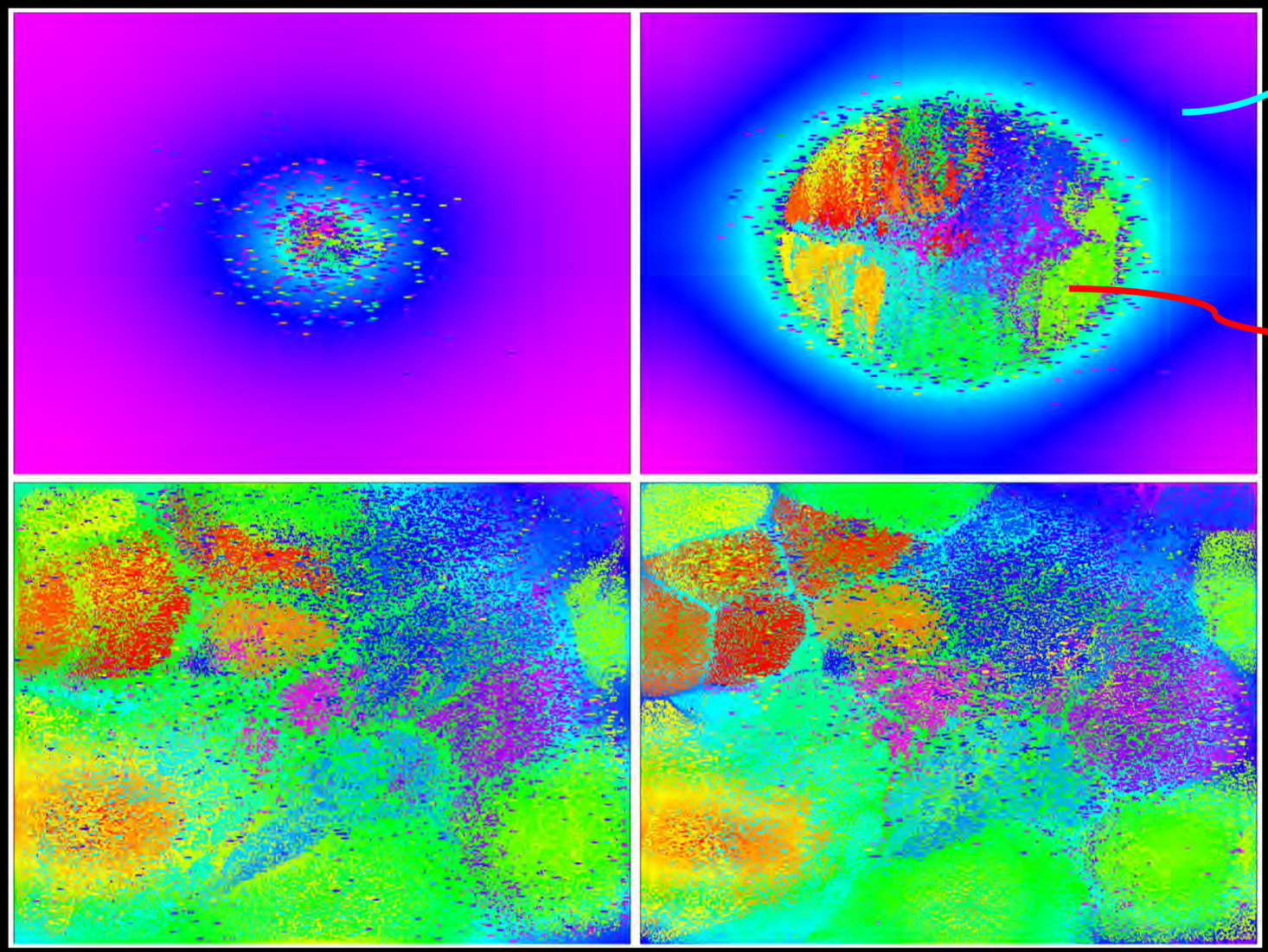


FastPlace

[1] Experiments performed by Guilherme Flach

Evaluating the Quality of a Solution

A global placement algorithm based on Poisson Equation

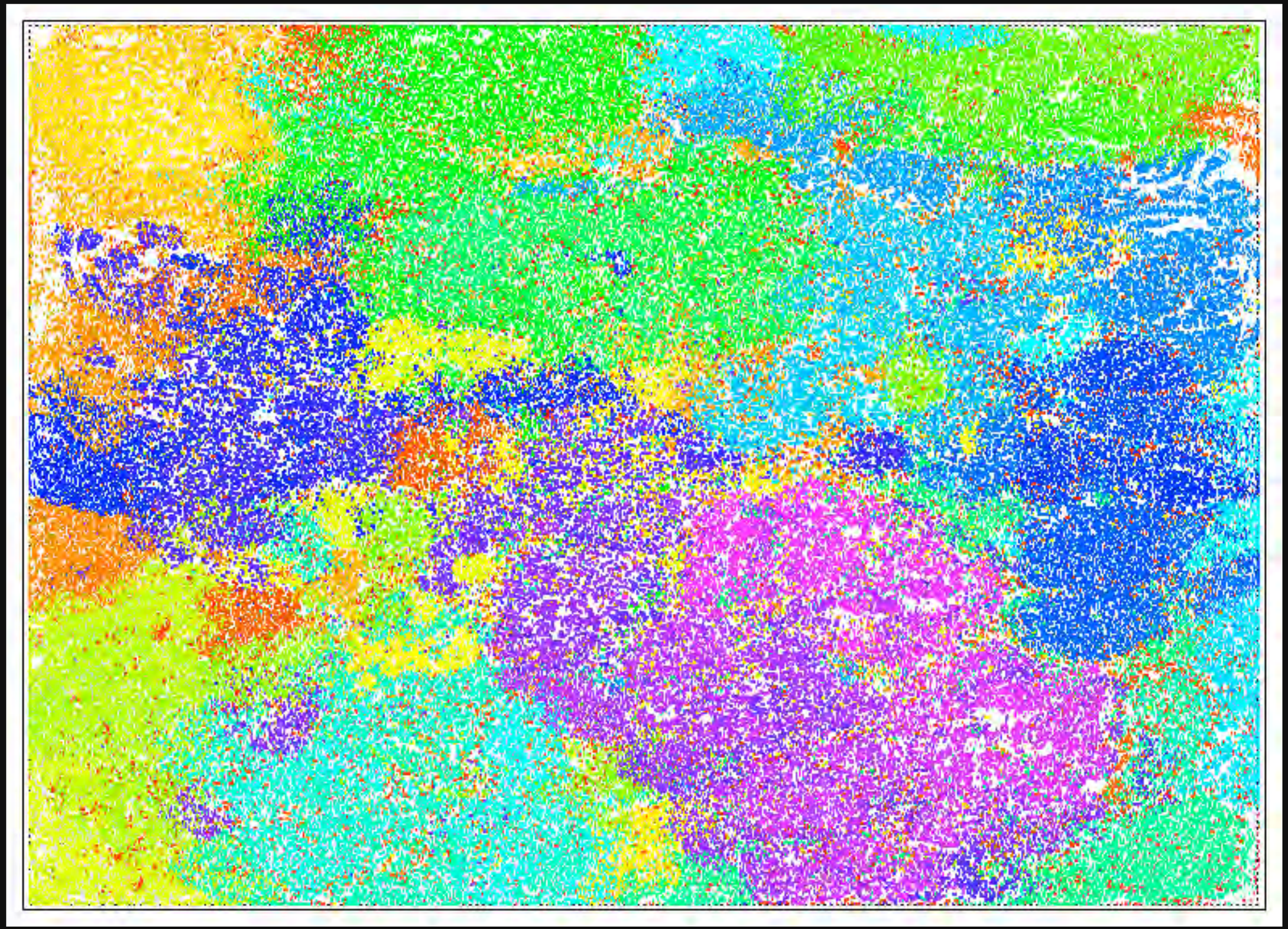


The **background** is a **heatmap** indicating **congestion**

Cells are colored like in the **previous example**

Placement of the IBM18 circuit using UFRGS tools

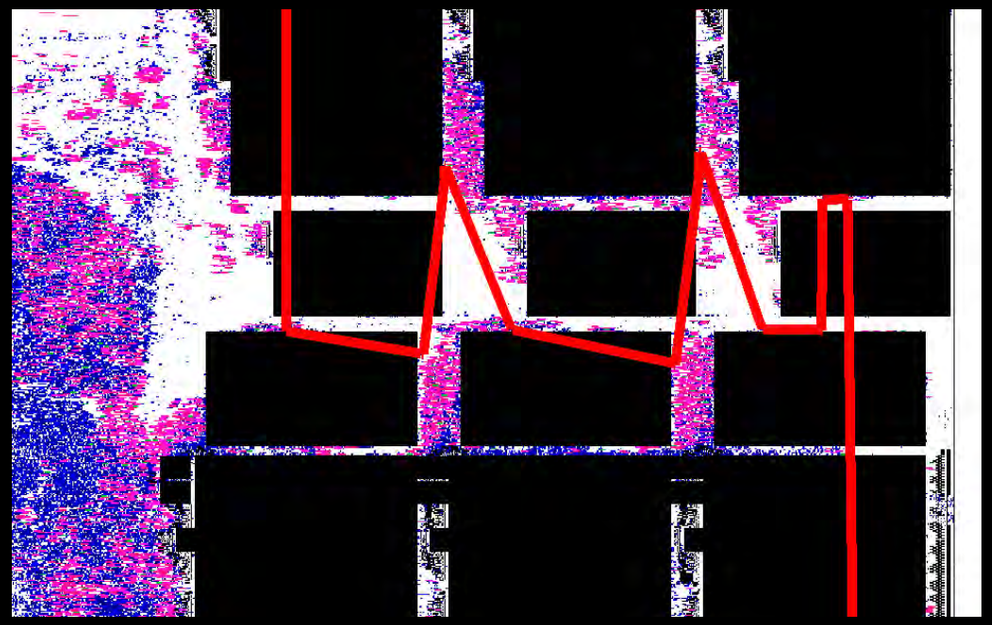
> 200 thousand logic cells



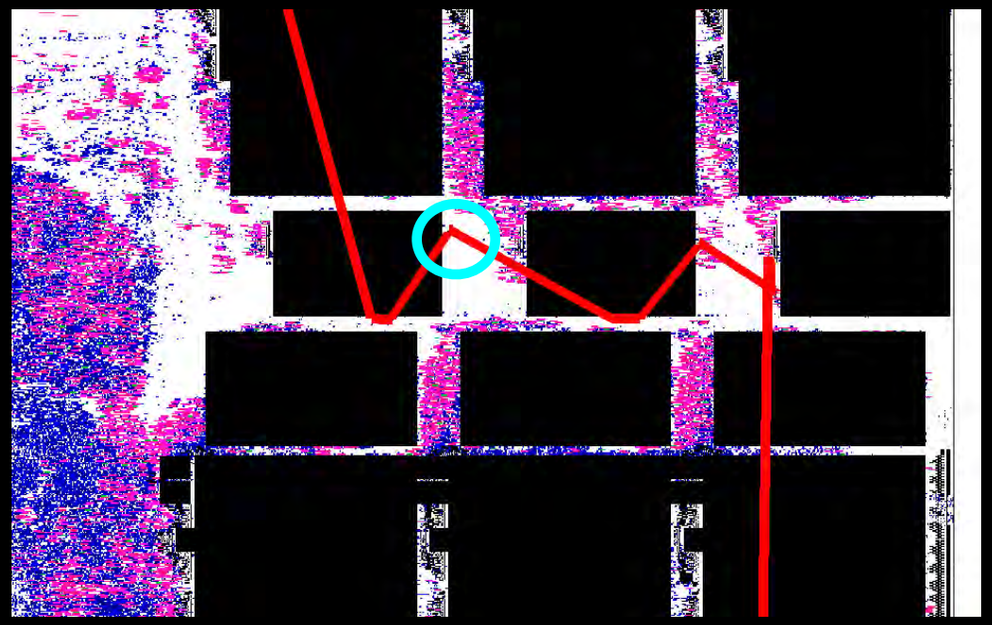
Design Debug and Improvement

Critical path smoothing for timing-driven placement

Initial solution

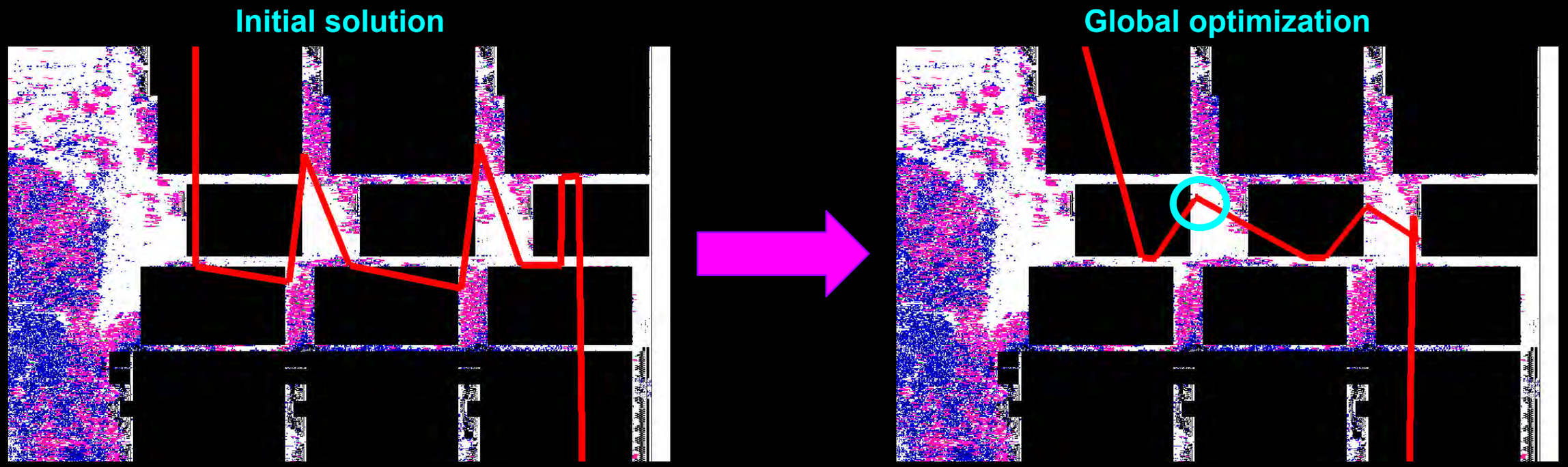


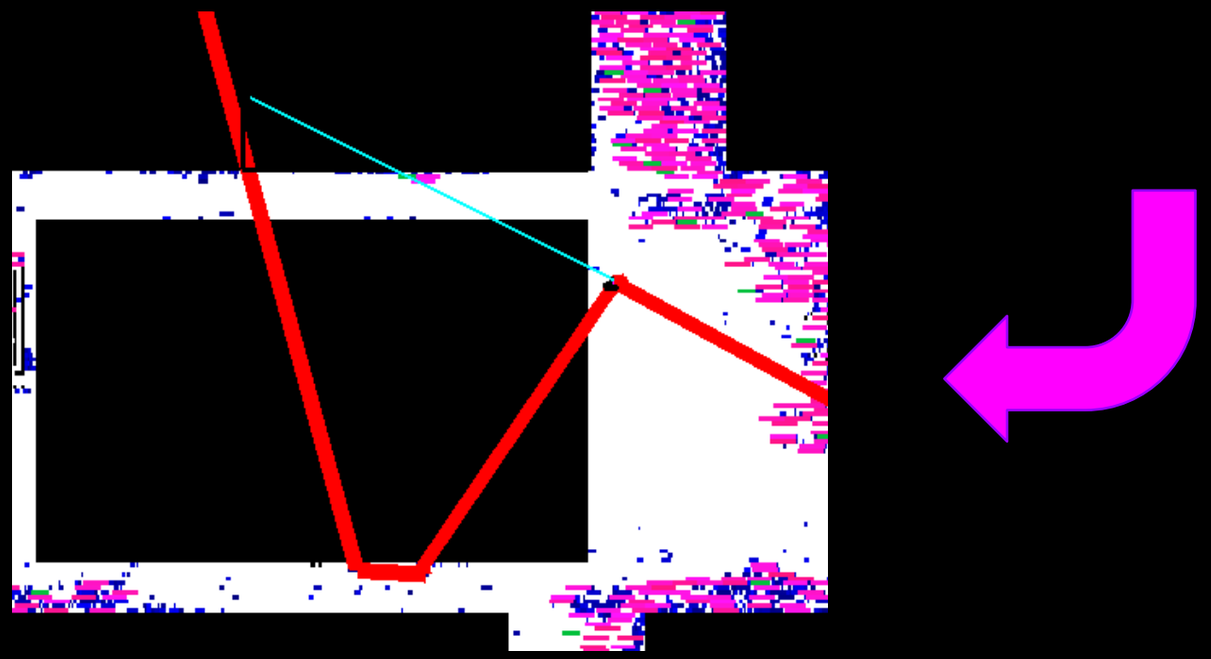
Global optimization



Why not further aligned?

Critical path smoothing for timing-driven placement





Netlist Placer Canvas Coloring Testing Actions

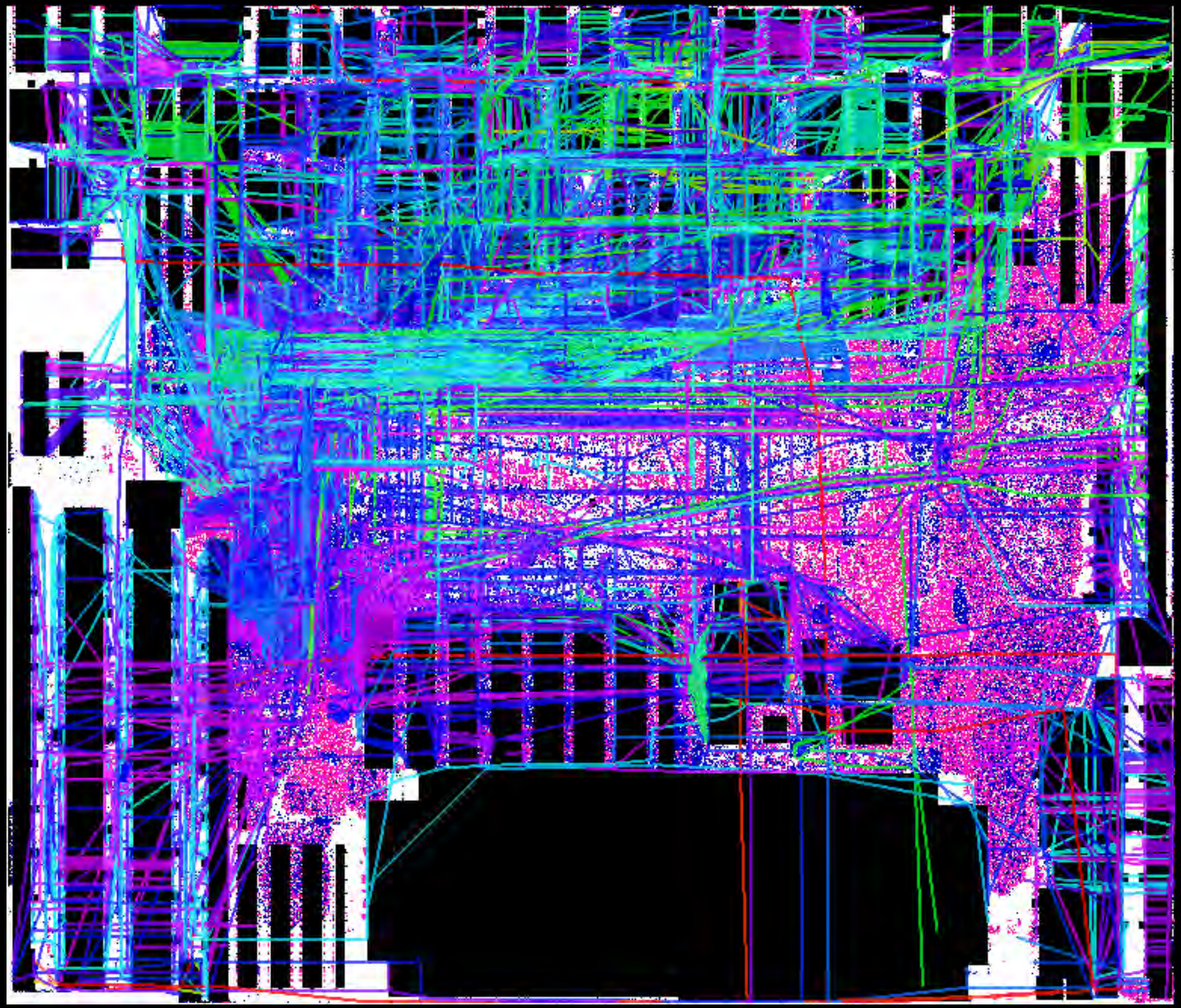
Design Canvas Opto Report

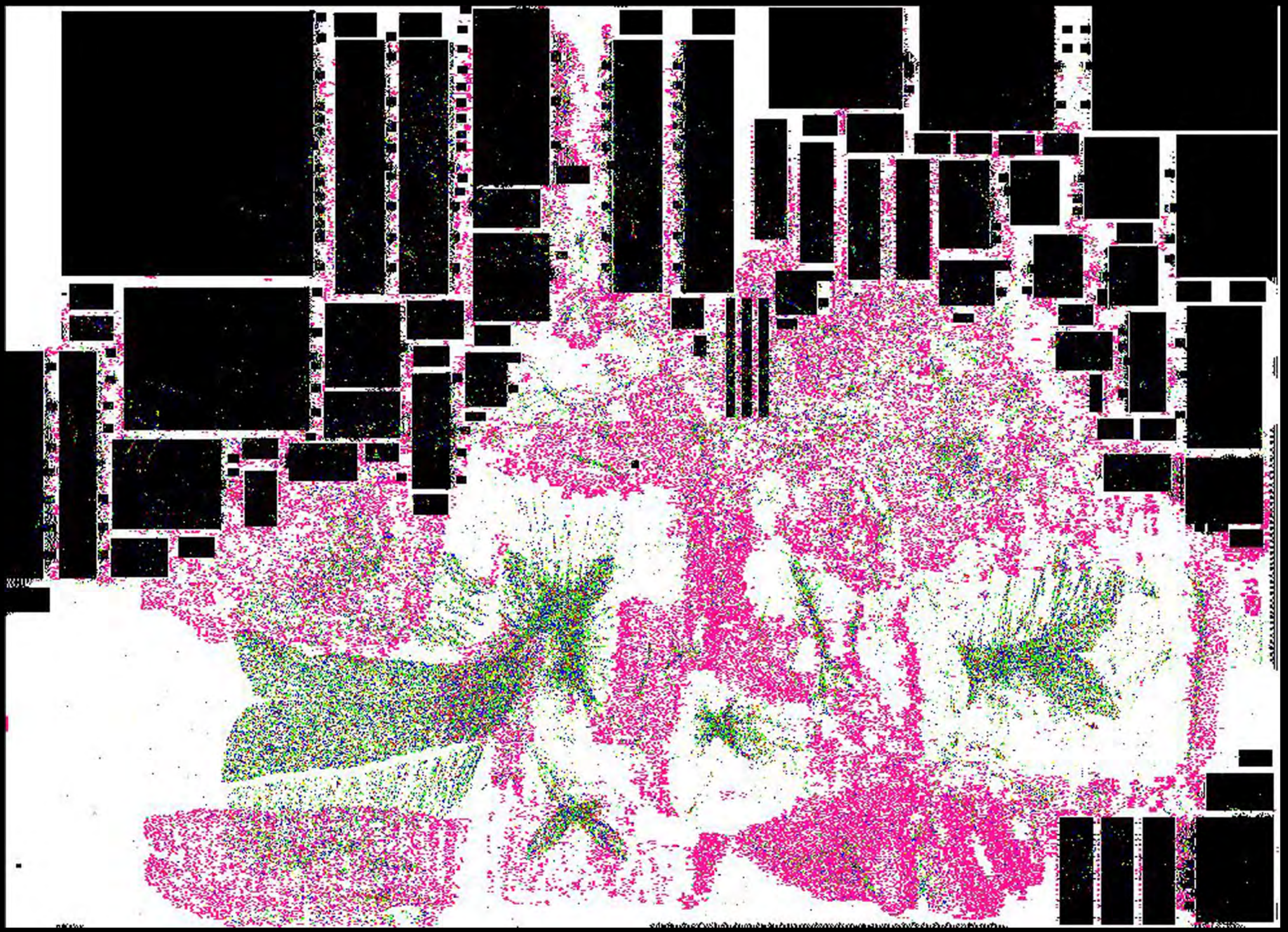
Search

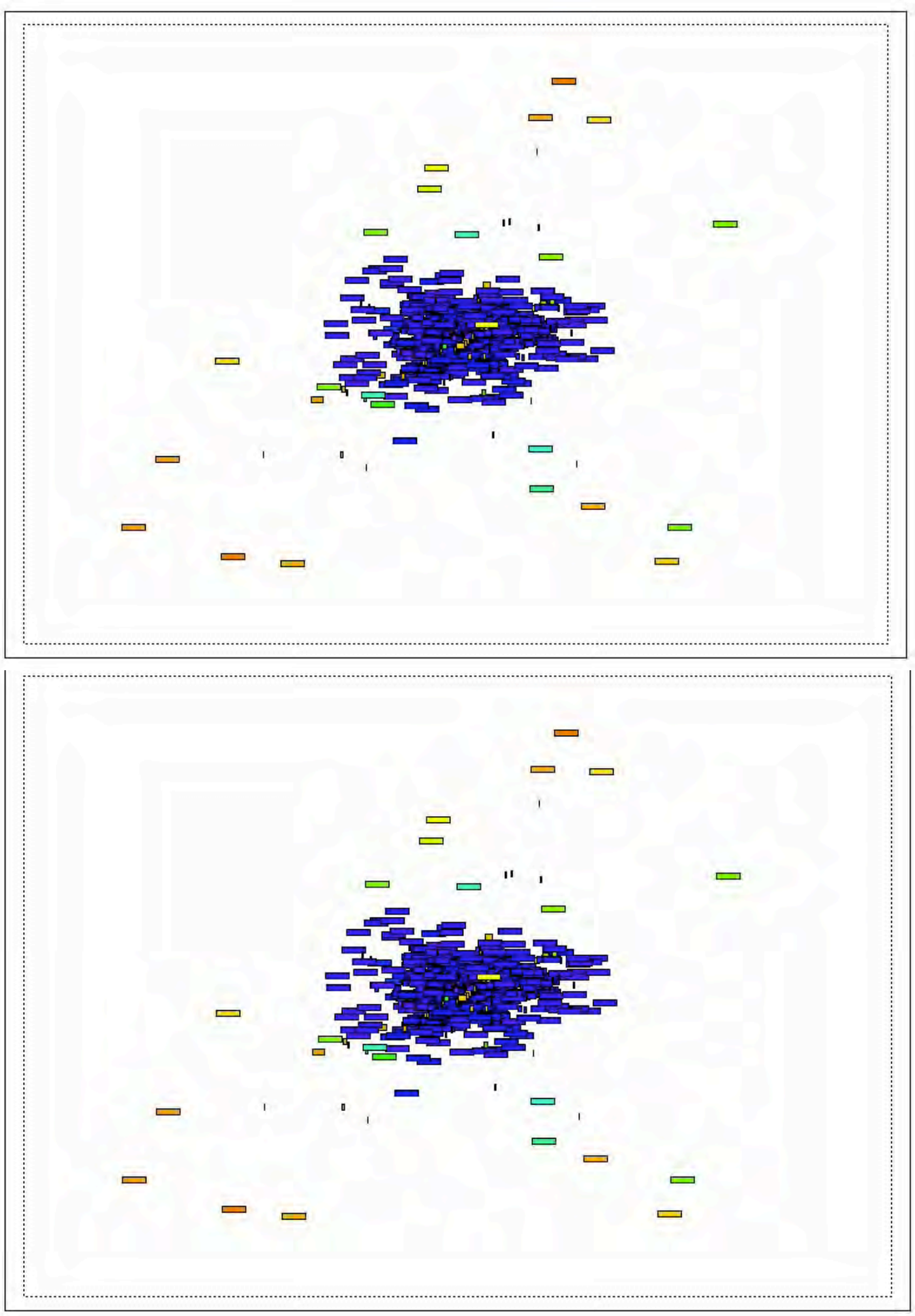
Cell

Name
LibCell
Placement
X
Y
Fixed (Current
Fixed (Original
Legalized
Dimension
Width
Height
Timing (Early)
Criticality (E)
Centrality (E)
Timing (Late)
Criticality (L)
Centrality (L)
Delay (Max)
Wire Delay (Ma
Rdrive (Max)
Load (Max)

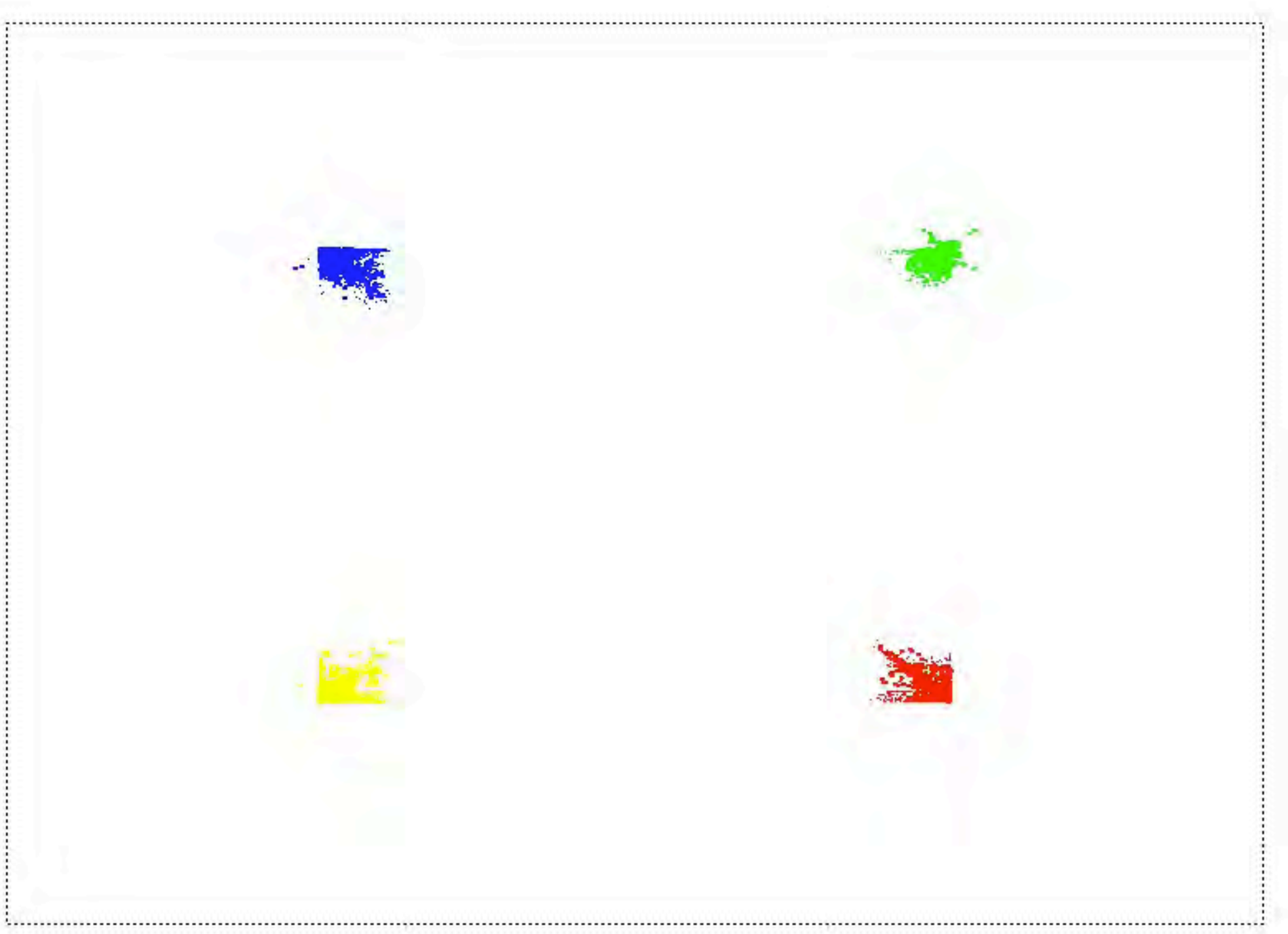
StWL: 1.91762e+11 ABU Penalty: 0.00191 Quality Score: 0.00000





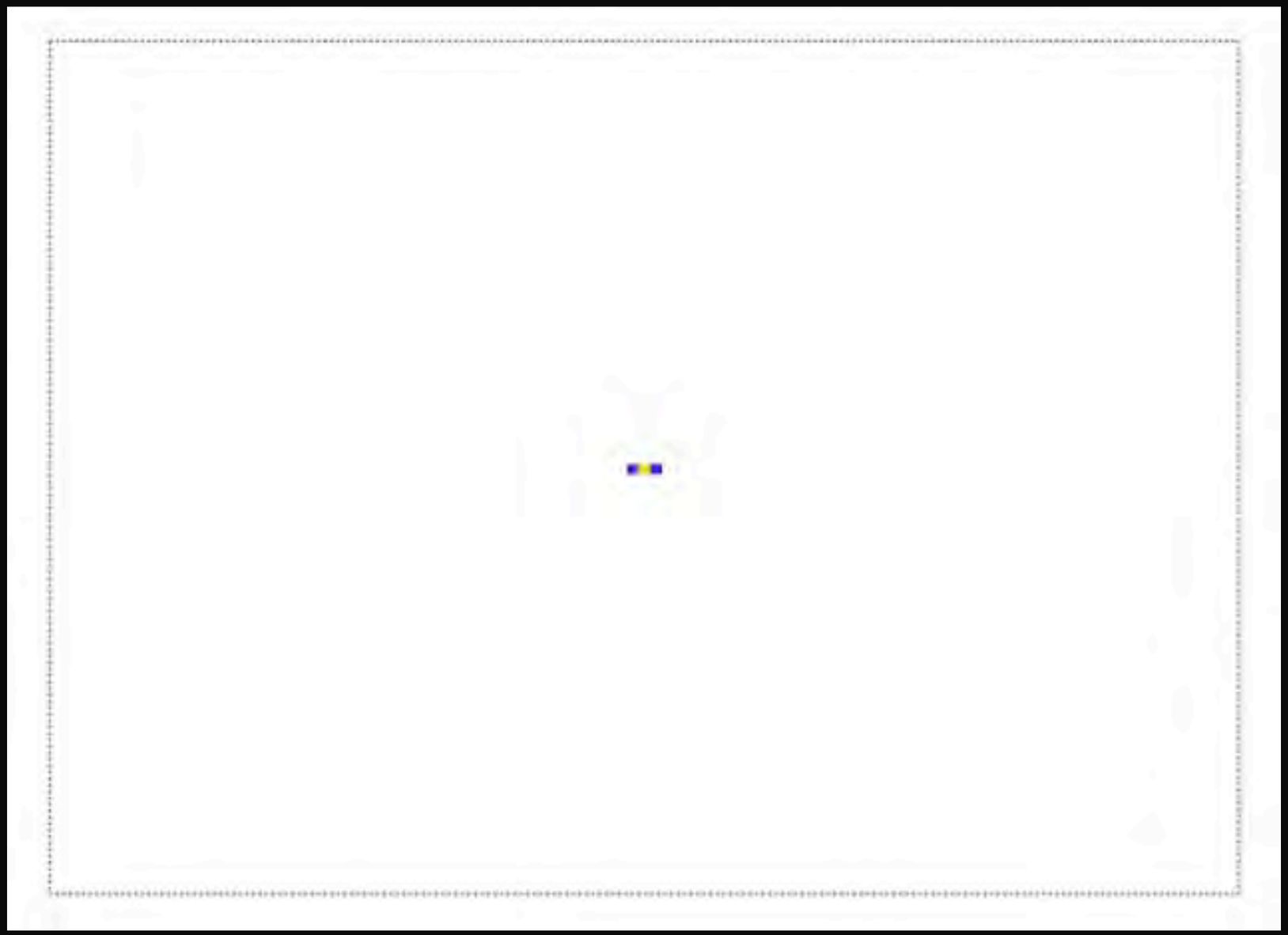


Placement using PlaceDL



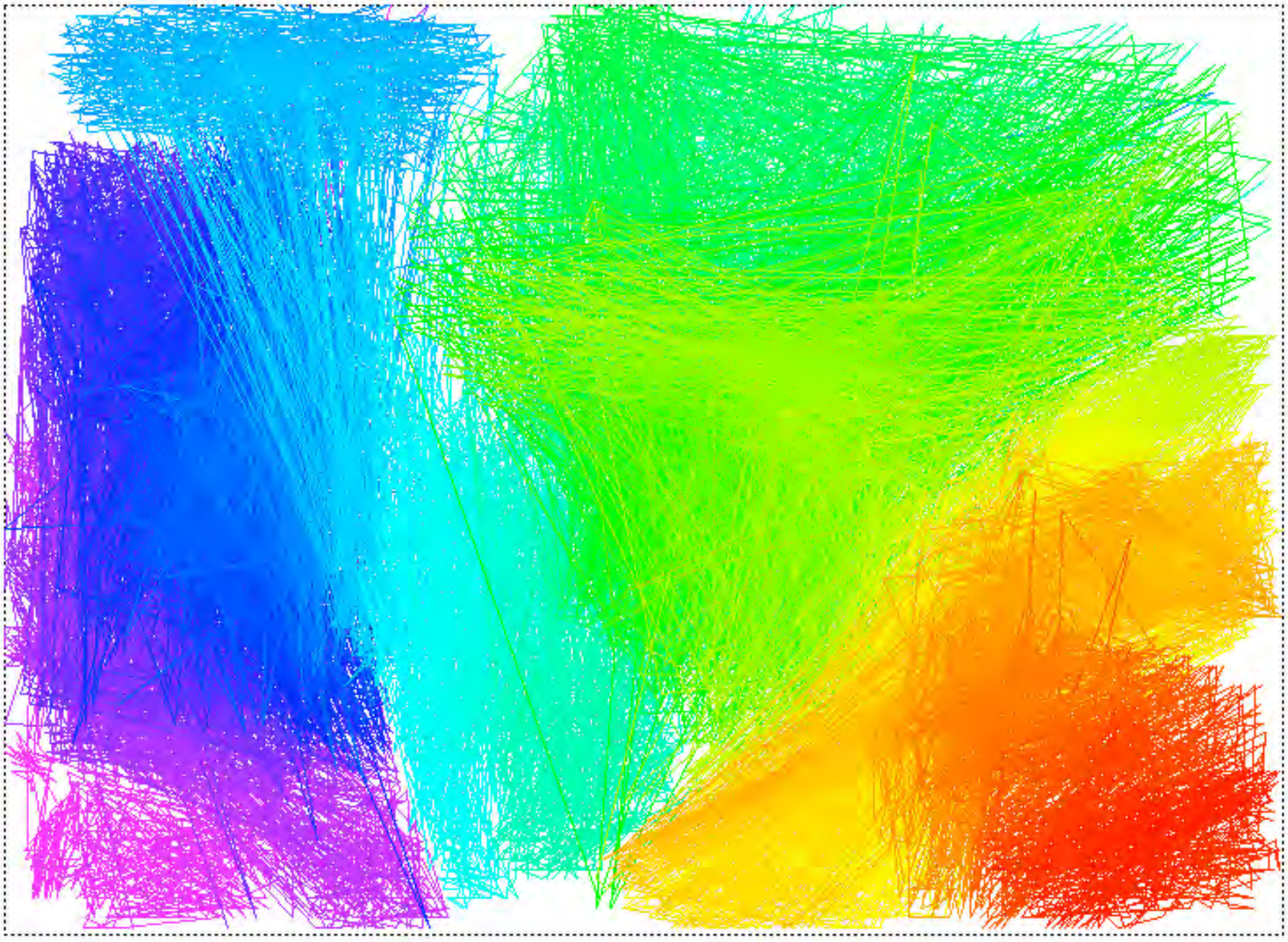
Placement of IBM1

experiment2



Routing Colors

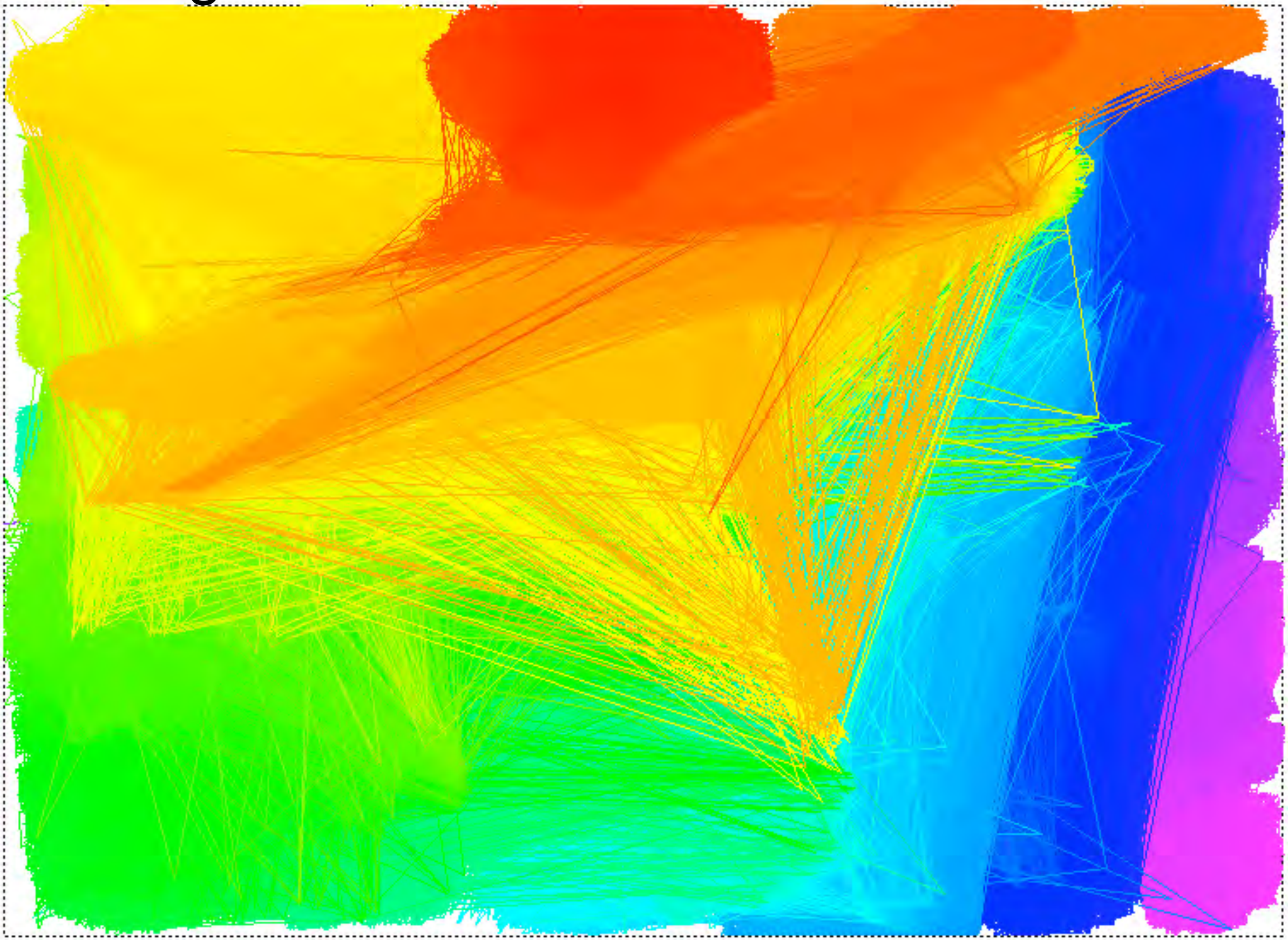
OBS: This and other pictures will be presented at the DAC ART SHOW, Austin, Texas, June 6-9, 2016



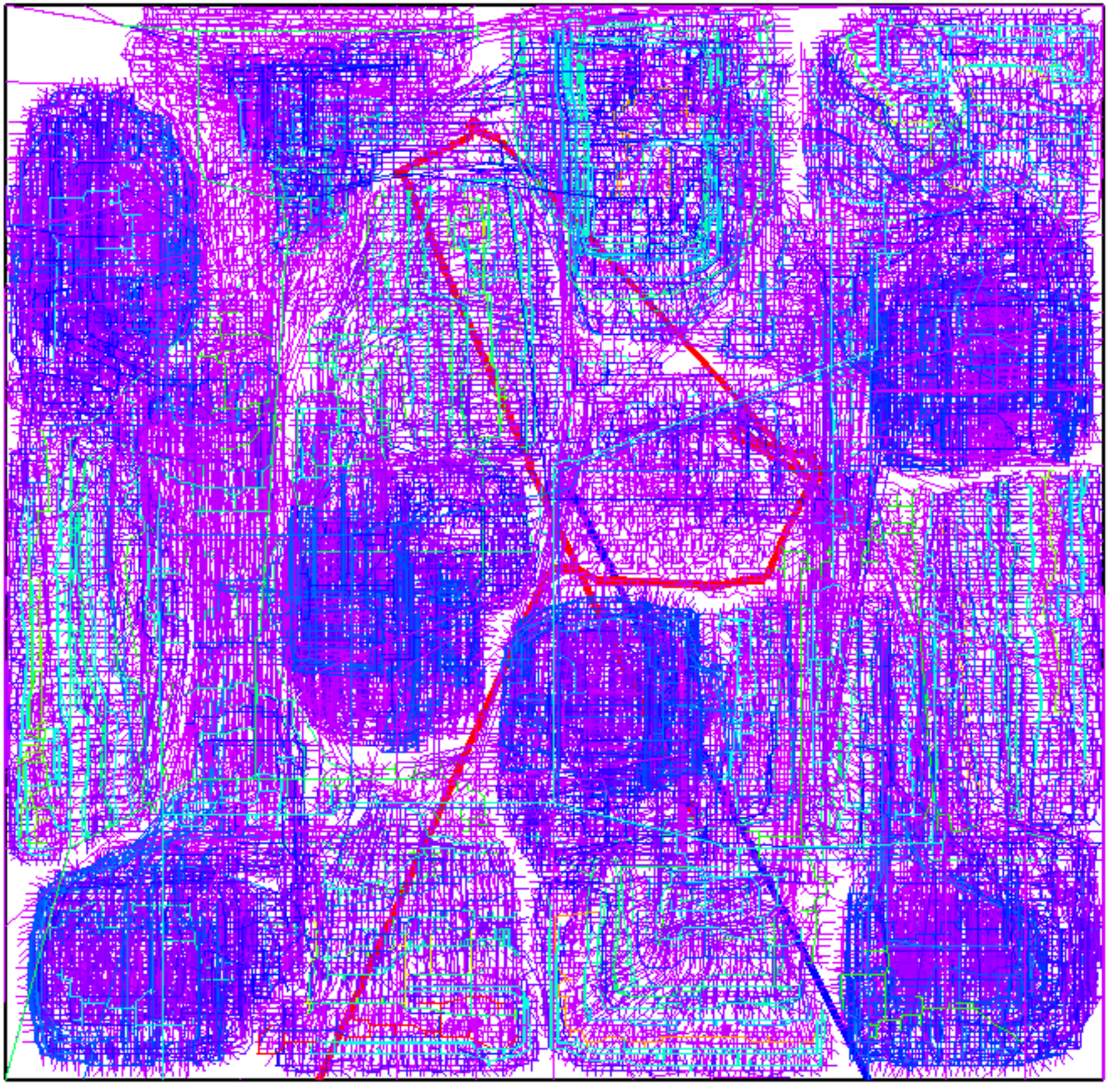
IBM1

The logic cells were ordered according to the Fiedler Vector (autovector associated to the second smaller autovalue) of the connective matrix of the graph and a line was drawn between pairs of adjacent cells.
The color of the line is a gradient between the colour of the initial cell and the color of the sink cell.
The color of the cells were obtained by mapping in a temperature map the value of the cell in the Fiedler Vector.

Routing Colors

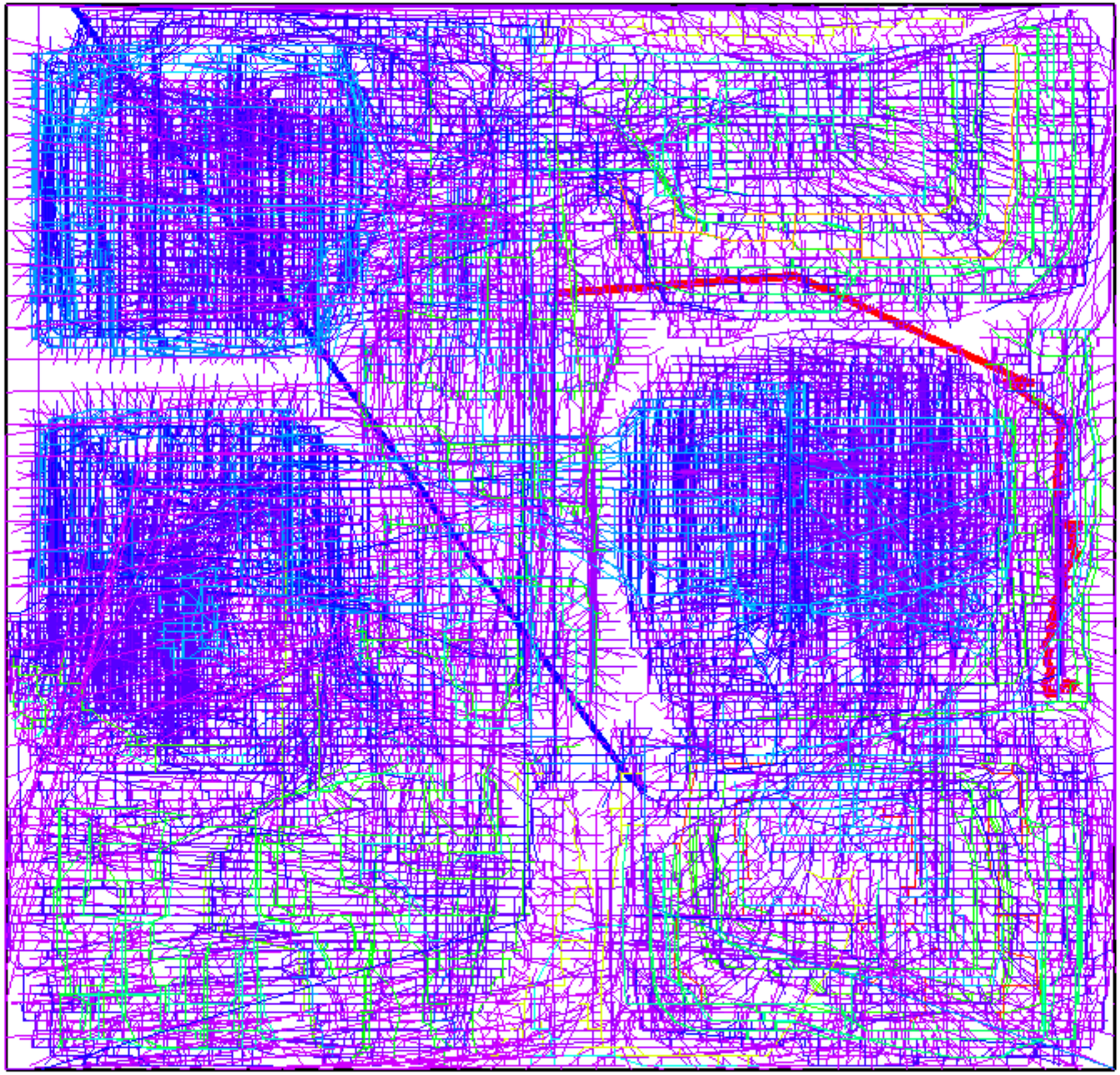


Routing Estimation (b18)



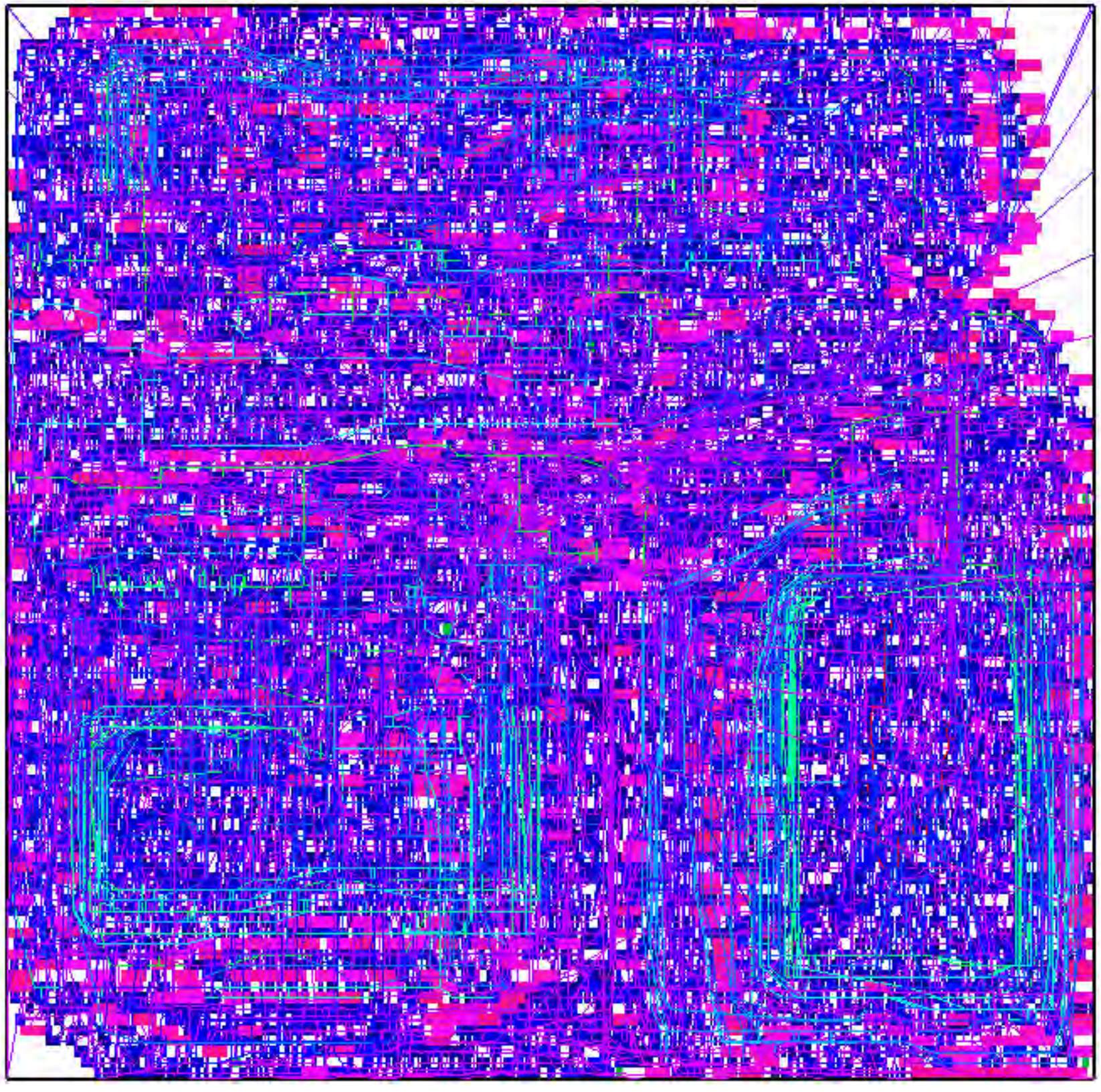
by Mateus Fogaça

Routing Estimation (b17)



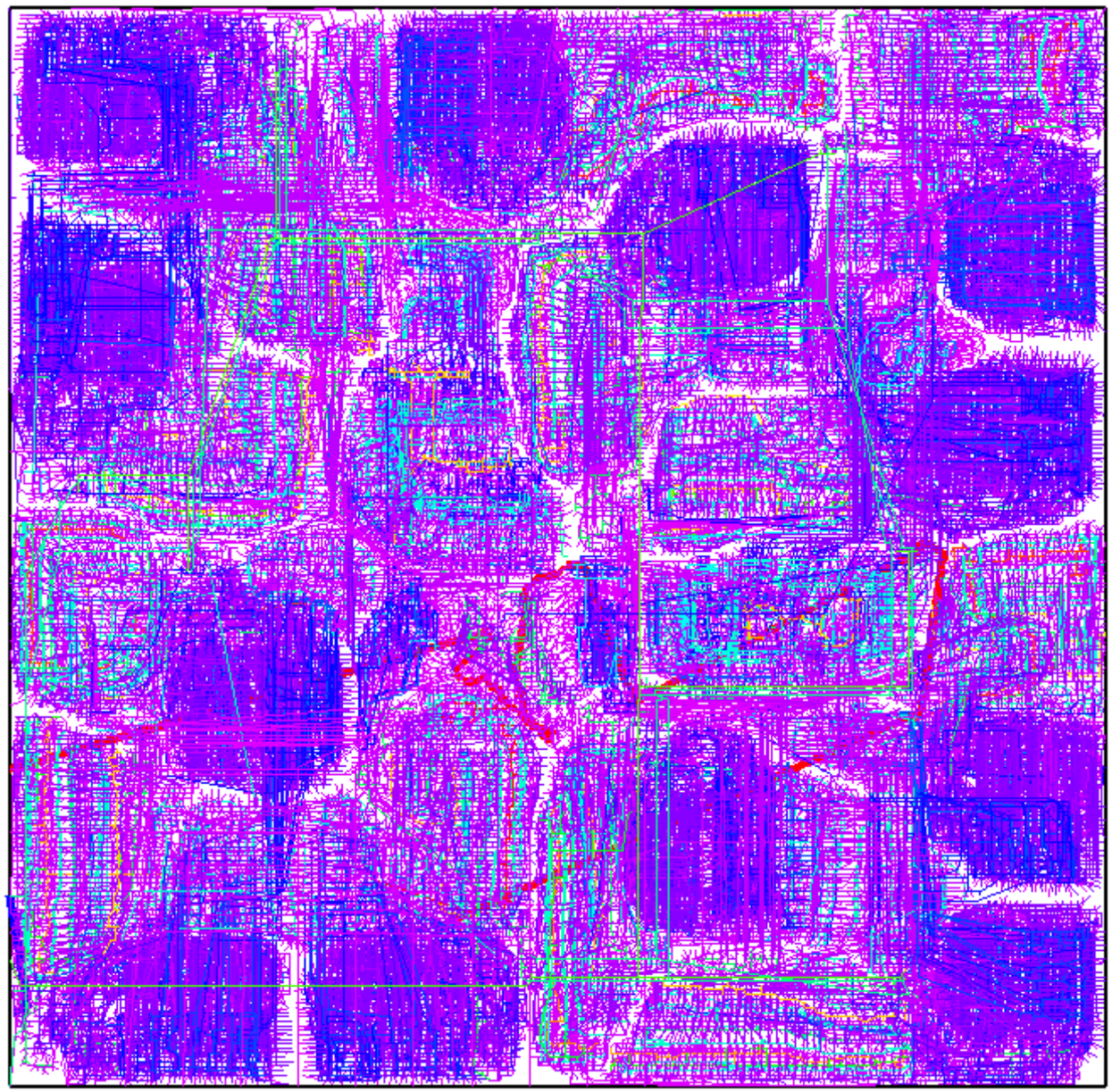
by Mateus Fogaça

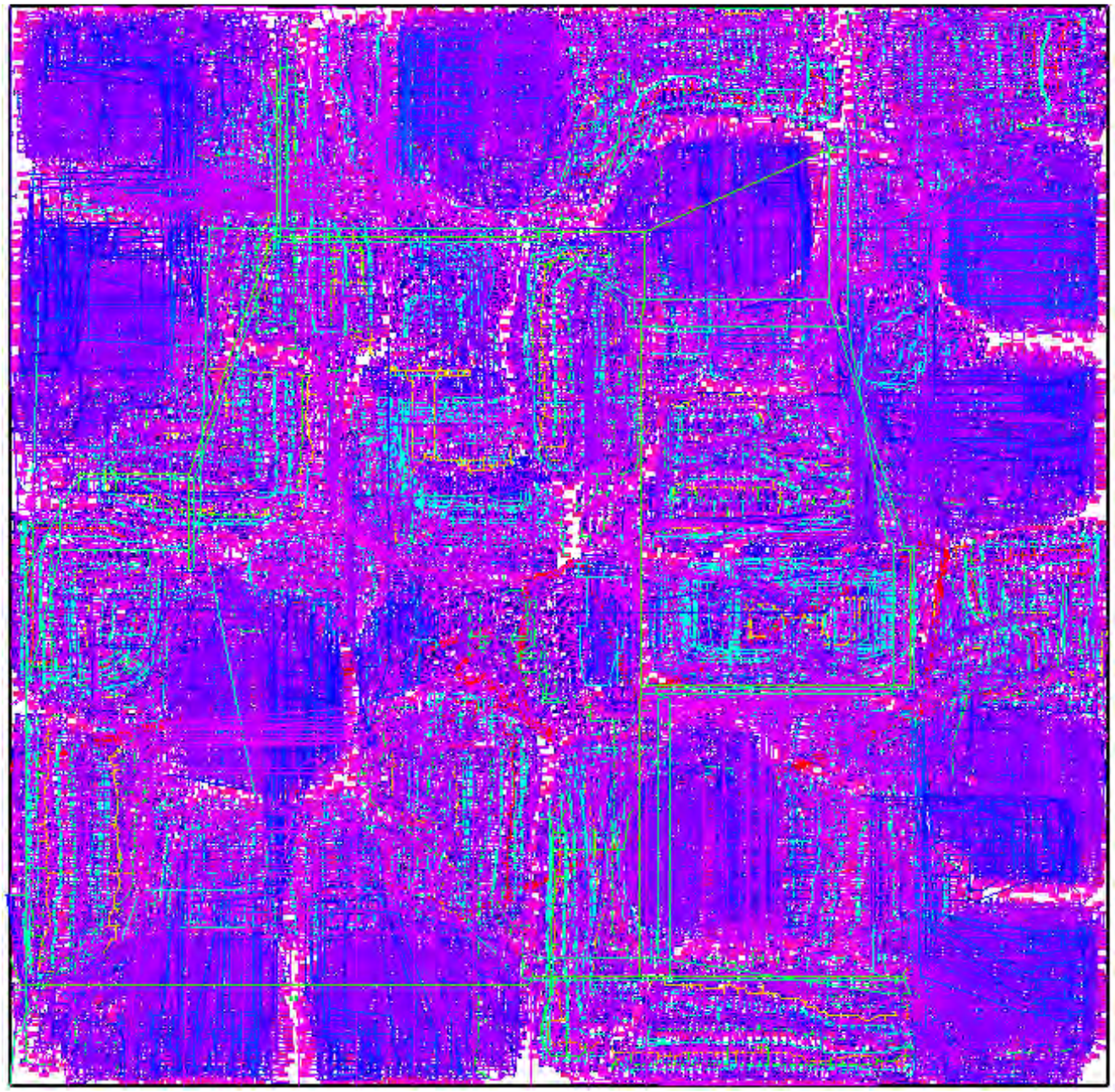
Routing Estimation (b22)



by Mateus Fogaça

Routing Estimation (b19)

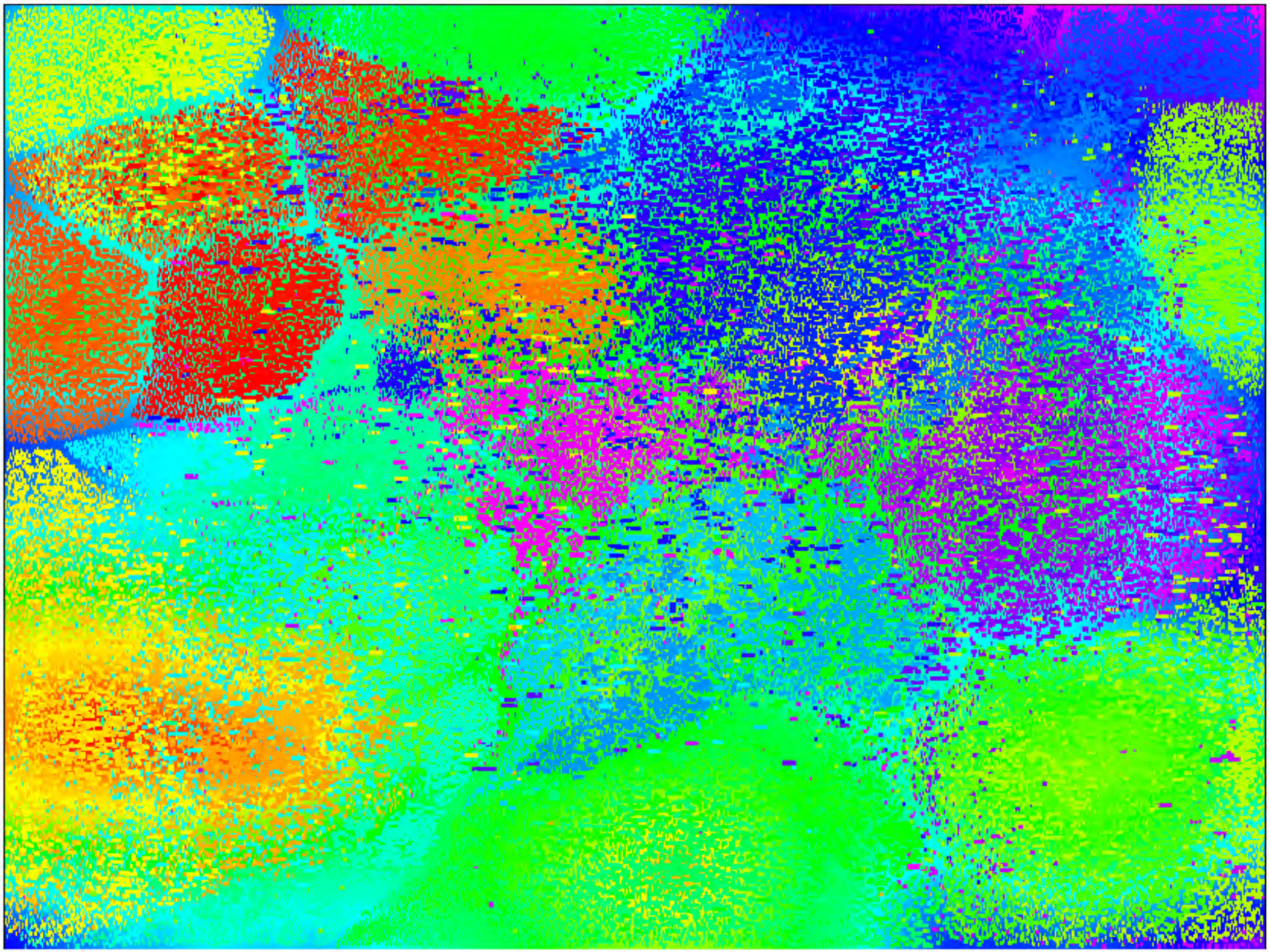




by Mateus Fogaça

DAC ART SHOW 2016

Applying Poisson equation with a quadratic approach to standard cell placement.



DAC 2017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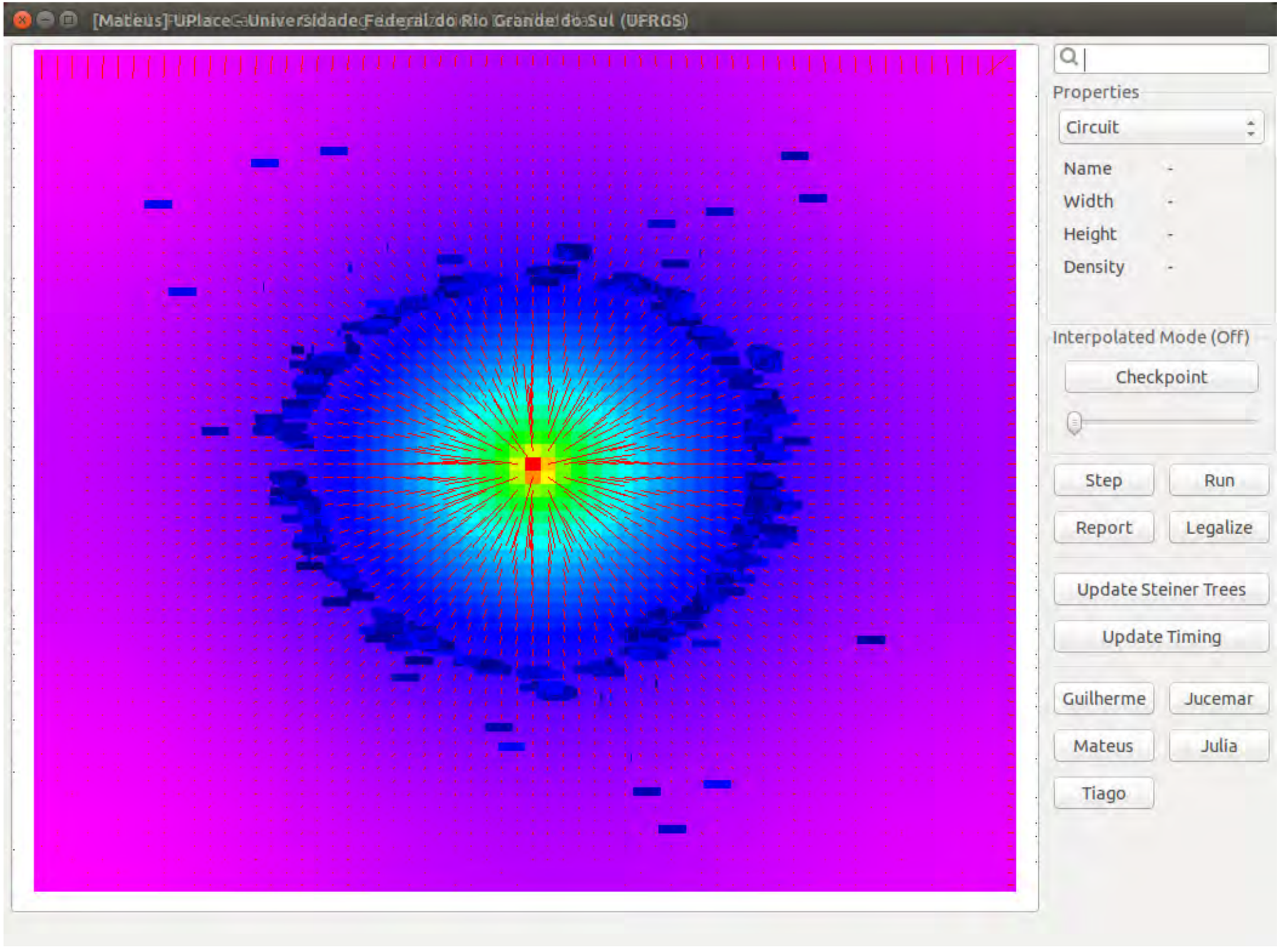
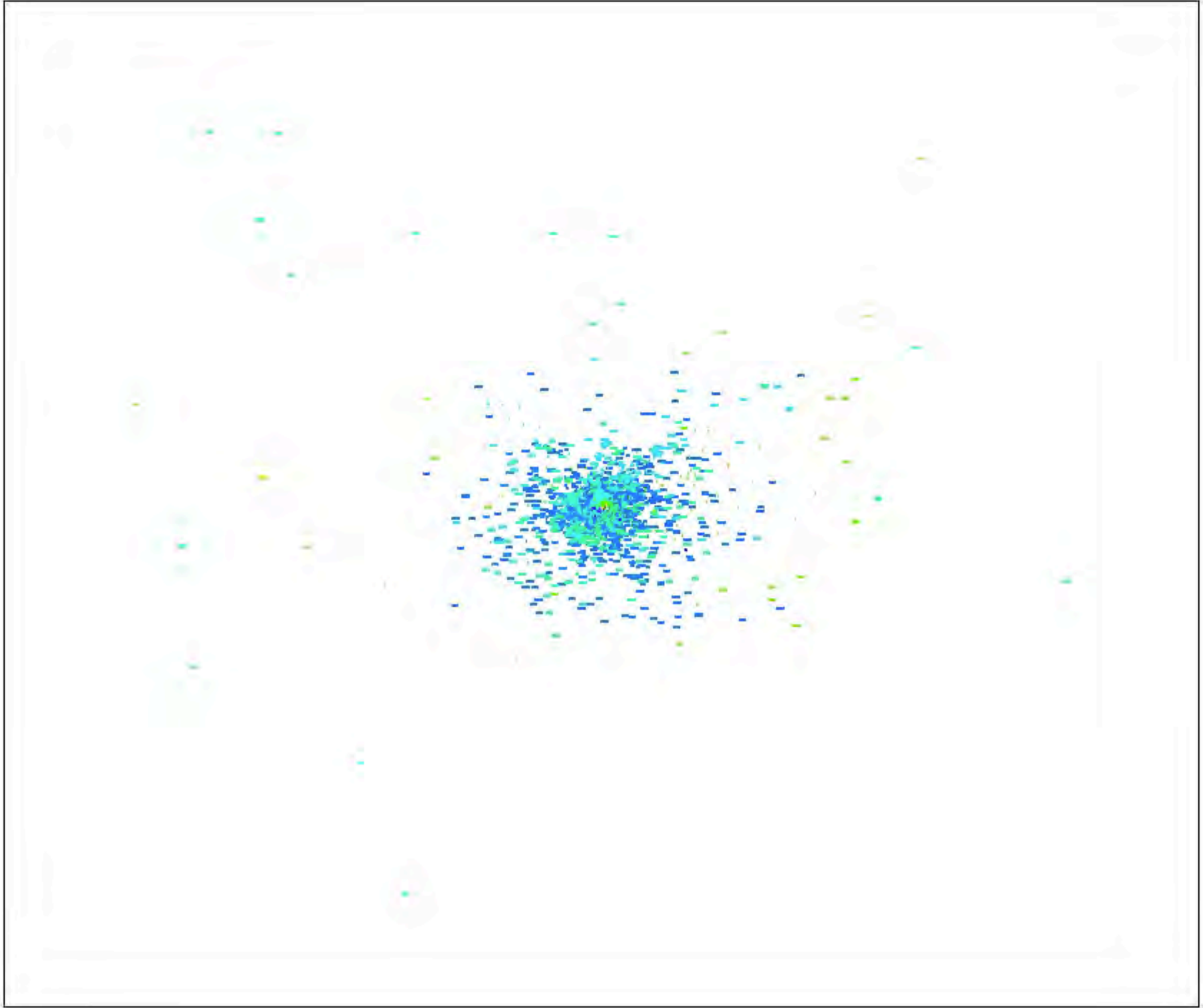
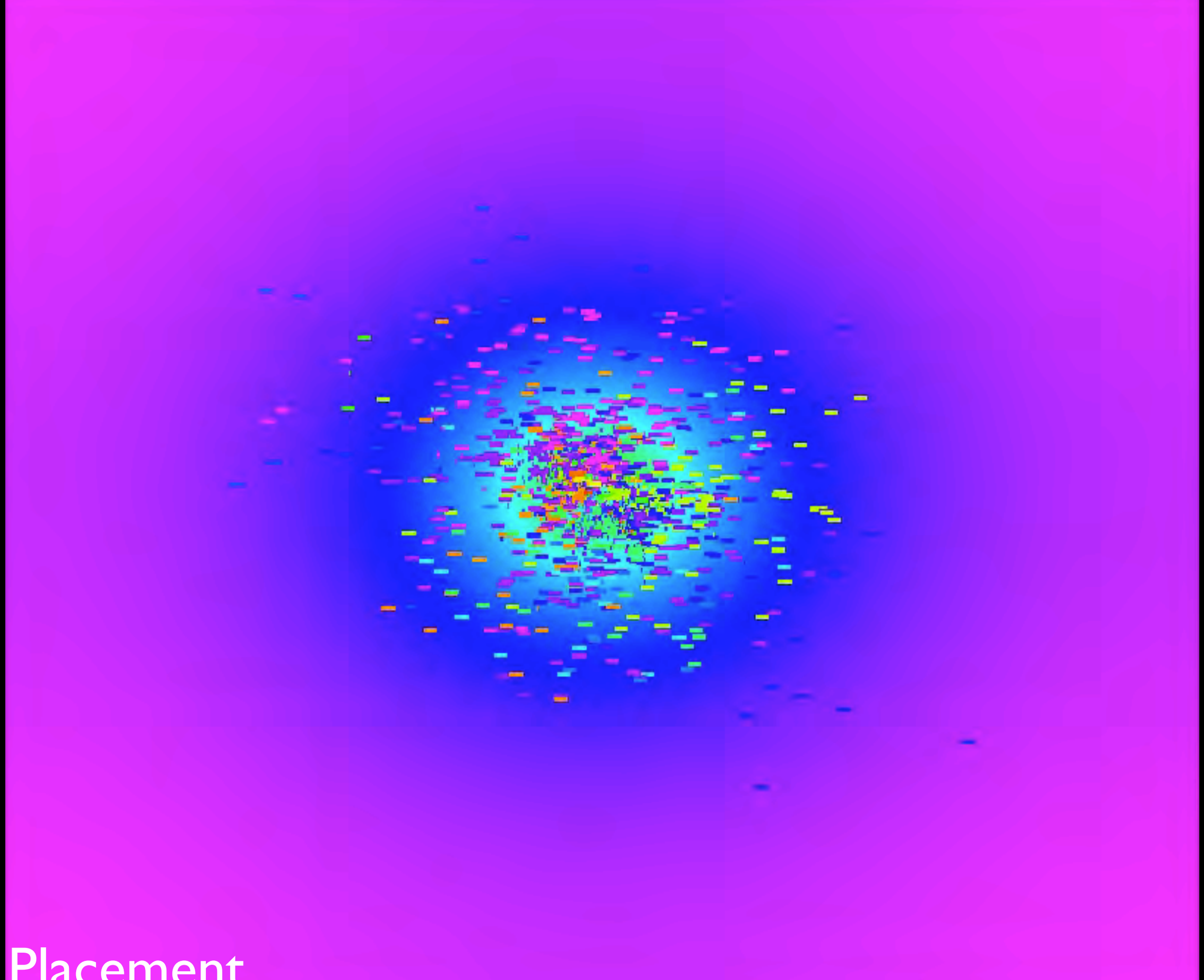

[Mateus] UPlace - Universidade Federal do Rio Grande do Sul (UFRGS)
Properties
Circuit
Name -
Width -
Height -
Density -
Interpolated Mode (Off)
Checkpoint
Step
Run
Report
Legalize
Update Steiner Trees
Update Timing
Guilherme
Jucemar
Mateus
Julia
Tiago





Placement

ISPD - International Symposium on Physical Design
Discrete Gate Sizing Contest 2012

organized by Intel

Second Place in one ranking (result metric)
First Place in the second ranking (that included running time)

Tiago Reimann, Guilherme Flach, Gracieli Posser
Jozeanne Belomo, Marcelo Johann, Ricardo Reis

UFRGS

ISPD - International Symposium on Physical Design
Discrete Gate Sizing Contest 2013

organized by Intel

First Place in the Primary Metric Ranking

UFRGS

ICCAD Contest 2014
First Prize

Incremental Timing-Driven Placement

Team:
Guilherme Flach, aluno de doutorado,
Jucemar Monteiro, aluno de mestrado,
Julia Puget, bolsista IC
Mateus Fogaça, graduando na FURG,

Advisors:
Marcelo Johann
Ricardo Reis
Paulo Butzen (FURG)

UFRGS

ICCAD Contest 2015
Second Place

Incremental Timing-Driven Placement

Team:
Guilherme Flach, PhD student
Jucemar Monteiro, PhD student
Mateus Fogaça, PhD student
Tiago Reimann, PhD student

Advisors:
Marcelo Johann
Ricardo Reis

IEEE/ACM ICCAD 2015 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN 34th Edition

UFRGS

Conclusions

The use of visualizations tools is more and more important to improve:

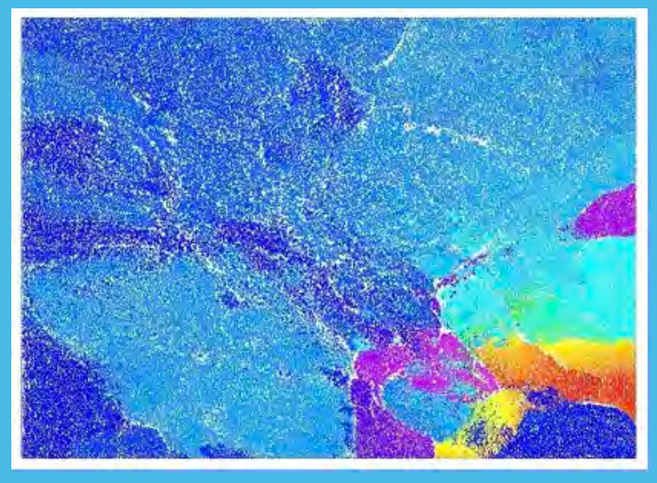
Algorithm behaviours
Evaluation of the solution quality
Design debug
Design improvement

IEEE CASS Seasonal School on

Physical Design Automation

Porto Alegre, Brazil
July 31 to August 5, 2017

www.inf.ufrgs.br/cass/pda/



The 2017 Seasonal School on Physical Design Automation aims to offer a set of talks on key topics of physical design automation of integrated circuits in modern and upcoming technologies. It should represent current and future challenges that are faced by industry and academia for the implementation of ever more complex circuits and systems. We want to promote discussion on hot topics and cover fundamental algorithms and computational methods in the area, so that the attendance can leverage their comprehension and capabilities, while also attracting new students and researchers to the right problems. The courses will be given by prominent international researchers with extensive expertise in their fields. Associated to the school, a book will be organized and published by an internacional publisher.

The School's technical program will include 8 courses of 2h40min each, divided into two parts of 1h20min each, with a coffee break. There will be a panel each day to involve participants into discussions related to the subjects covered. In the afternoon coffee break, there will be a poster sessions related to the school topics. The corresponding call for posters is available in the webpage.

THE MAIN TOPICS TO BE COVERED BY THE SCHOOL WILL INCLUDE:

Global and Detailed placement
Gate sizing
Routing and routability
Tools for 3D architectures
Layout manufacturability
Clock routing buffer/wire sizing
Machine Learning for EDA
Layout Design Automation

Some of the speakers are:

Andrew Kahng, UCSD, USA
William Swartz, TimberWolf Systems and UT Dallas, USA
Laleh Behjat, Univ. Calgary, Canada
Patrick Madden - SUNY Binghamton, USA
Ulrich Brenner - University of Bonn, Germany
Evangeline Young - CUHK, Hong Kong
Mark Po-Hung Lin - NCCU, Taiwan
Patrick Groeneveld, Formerly Synopsys, USA

General Chair :Ricardo Reis, UFRGS, Brazil

Program Chairs
Patrick Madden, SUNY Binghamton, USA
Marcelo Johann, UFRGS, Brazil

Poster Session Chair: Jucemar Monteiro, UFRGS

Local Organization Chair
Mateus Fogaça, UFRGS
Jody Matos, UFRGS

IEEE CASS Liaison: Ricardo Reis, UFRGS, Brazil

IEEE CEDA Liaison: José Guntzel, UFSC, Brazil

IEEE CAS CEDA sigda SBC Brazilian Computer Society UFRGS PGMICRO inf Instituto de Informática UFRGS

LASCAS is the Flagship Conference of IEEE's Circuits and Systems Society in Latin America. Since its inception and first edition in 2010, LASCAS aims at presenting a high-quality forum for researchers and graduate students to present the advances of their work, amidst an international audience with experts from all over the world.

This 9th edition will take place in the port of Puerto Vallarta, a quaint city with many an interesting anecdote to tell, a gamut of restaurants to choose from, and spectacular views and breath-taking sunsets on the Pacific horizon.

The symposium will cover novel technical developments, and offer tutorial overviews on topics related to circuits and systems including, but not limited to:

- Analog and Digital Signal Processing
- Nanoelectronics and Gigascale Systems
- Cellular Neural Networks and Array Computing
- Neural Systems and Applications
- Circuits and Systems for Communications
- Nonlinear Circuits and Systems
- Graph Theory and Computing
- Electronic Design Automation
- Power Systems and Power Electronic Circuits
- RF Circuits and Systems
- Intelligent Sensor Systems
- Visual Signal Processing and Communications
- Multimedia Systems and Applications
- Life Science Systems and Applications
- Biomedical Circuits and Systems
- VLSI Systems and Applications
- Systems on Chip
- Electronic Testing
- Fault Tolerant Circuits

General Chairs:
Roberto S. Murphy, INAOE, Mexico
Arturo Sarmiento, INAOE, Mexico
Technical Program Chairs:
Ricardo Reis, UFRGS, Brazil
Maciej Ogorzalek, Jagiellonian University, Poland
Publications Chair:
Luis Hernández, INAOE, Mexico
Publicity Chair:
Ma. Teresa Sanz, INAOE, Mexico
Local Arrangements Chair:
Gabriela E. López, INAOE, Mexico

Call for Papers, Tutorials and Special Sessions:
Tutorial proposals: October 6, 2017
Special Session Proposal: October 6, 2017
Paper Submission: October 20, 2017
Notification of acceptance: November 21, 2017
Camera-ready: December 20, 2017
http://www-elec.inaoep.mx/~LASCAS18

The proceedings will be published by IEEE Xplore, and extended versions of a selection of the best papers will be invited to submit to a Special Issue of the IEEE TCAS 1, Transactions on Circuits and Systems 1, published by IEEE.

LASCAS2018 will be colocated with IBERCHIP 2018 and PRIME2018.

R9 IEEE CASS Flagship Conference

Best Papers will be invited to a special edition of the **IEEE Transactions on Circuits and Systems I (TCAS-I)**

LASCAS2019 - Armenia, Colombia
LASCAS2020 - San Jose, Costa Rica

35 years since 1983

SBCCI2018

31st SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN

CHIP IN THE PAMPA

Bento Gonçalves, Rio Grande do Sul, BRAZIL

August 27 to 31, 2017

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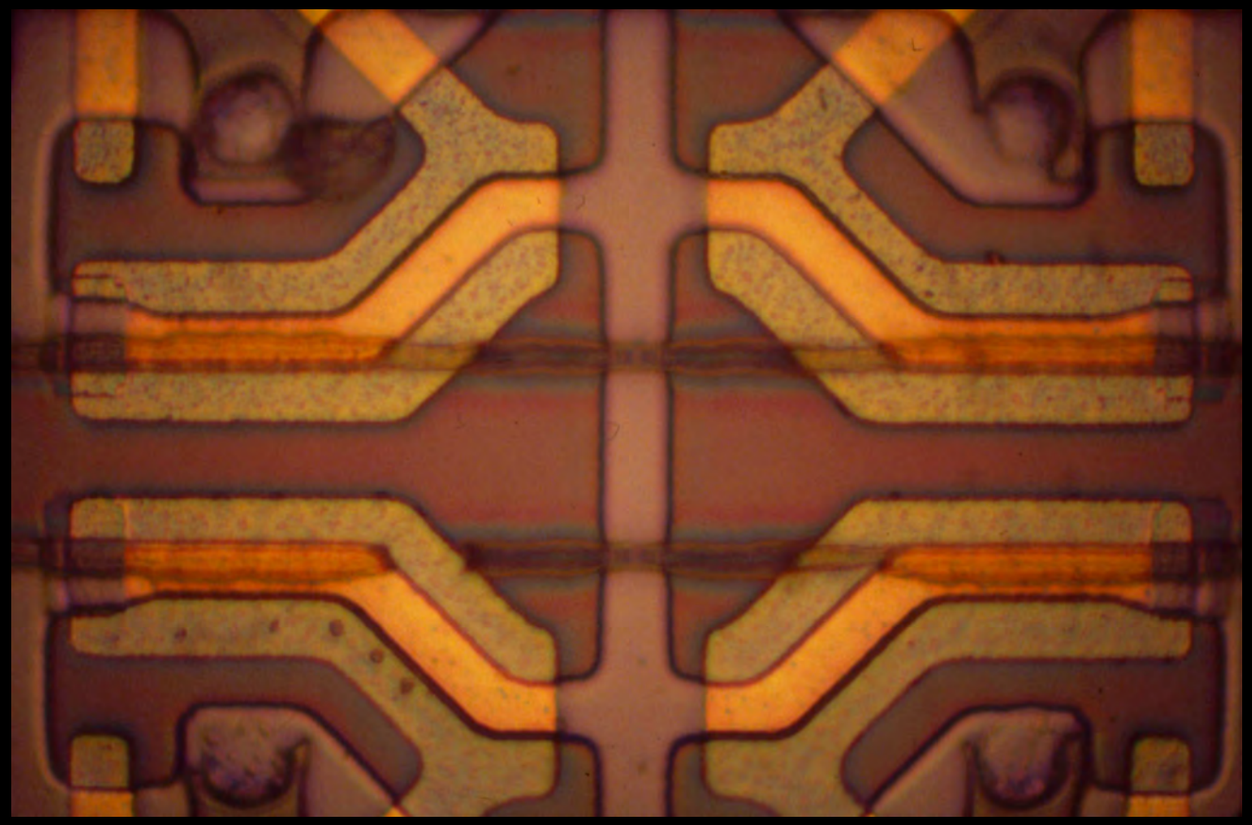
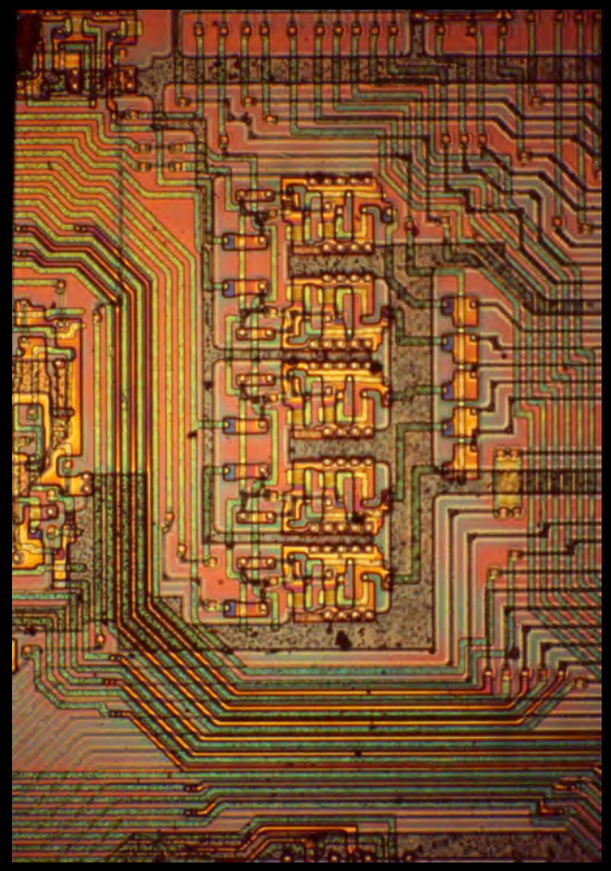
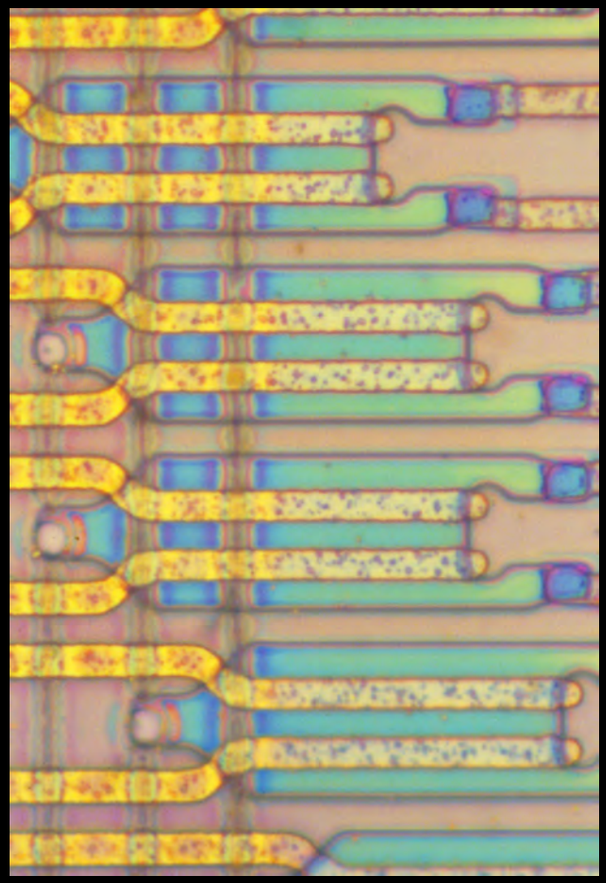
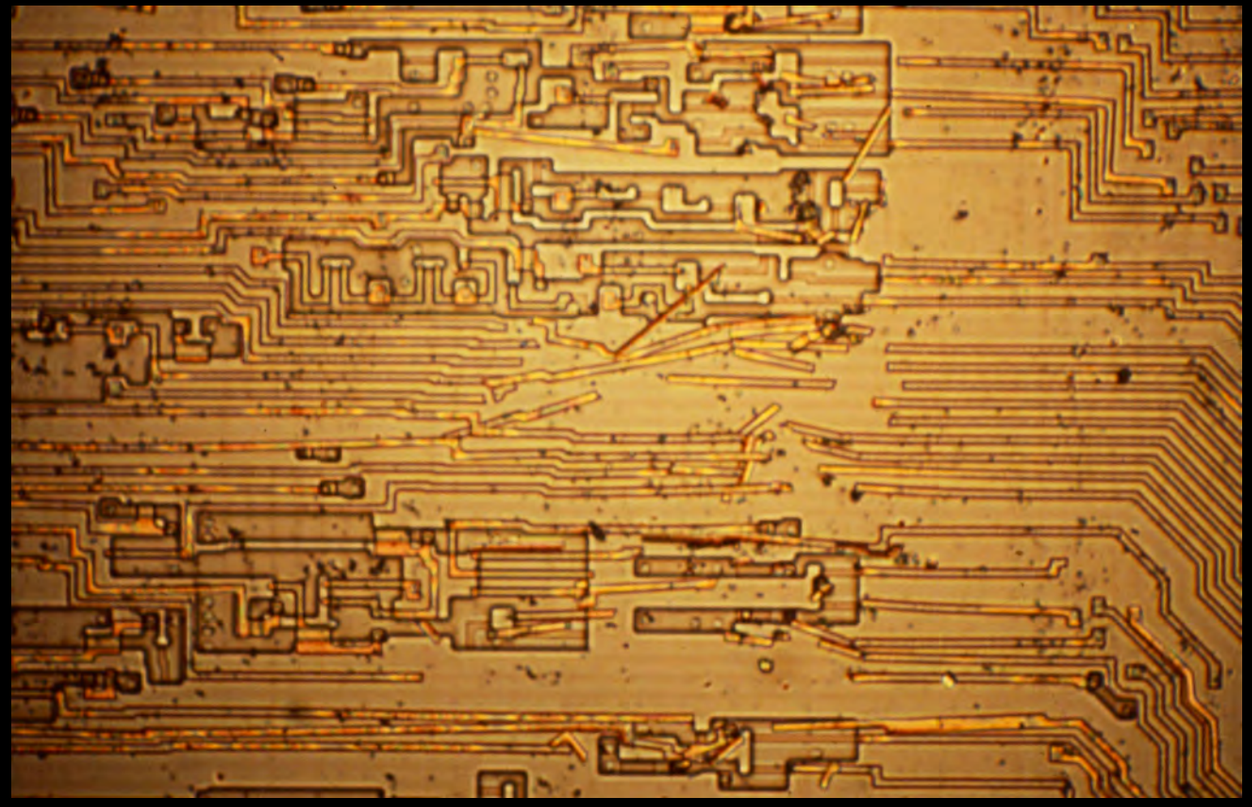
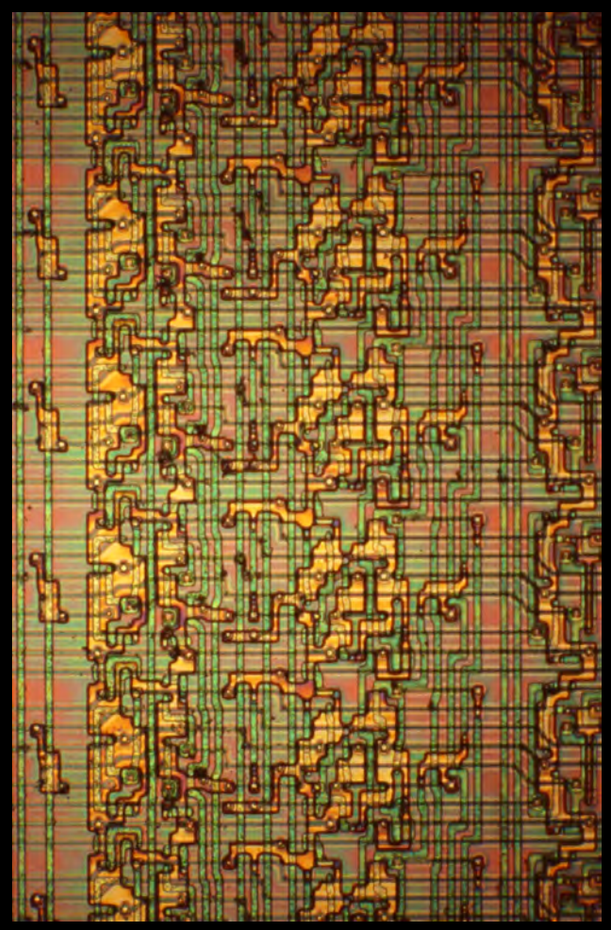
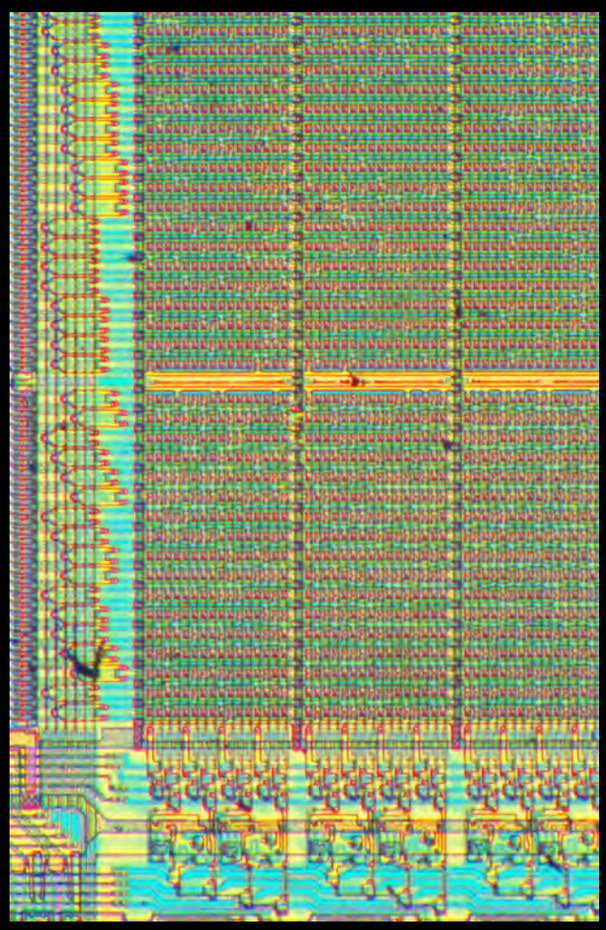
SBC Brazilian Computer Society · SB · IEEE · CAS IEEE CIRCUITS AND SYSTEMS SOCIETY · SIGDA · ifip · CEDA

Something Else

more photos at:

facebook.com/artchips1

Visualization Tools

Ricardo Reis, Mateus Fogaça, Guilherme Flach

UFRGS