Digital System Design

by
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Slide Set: 7
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Slide Set Overview

- Quizzes
  - Results
  - Answers

Quizzes

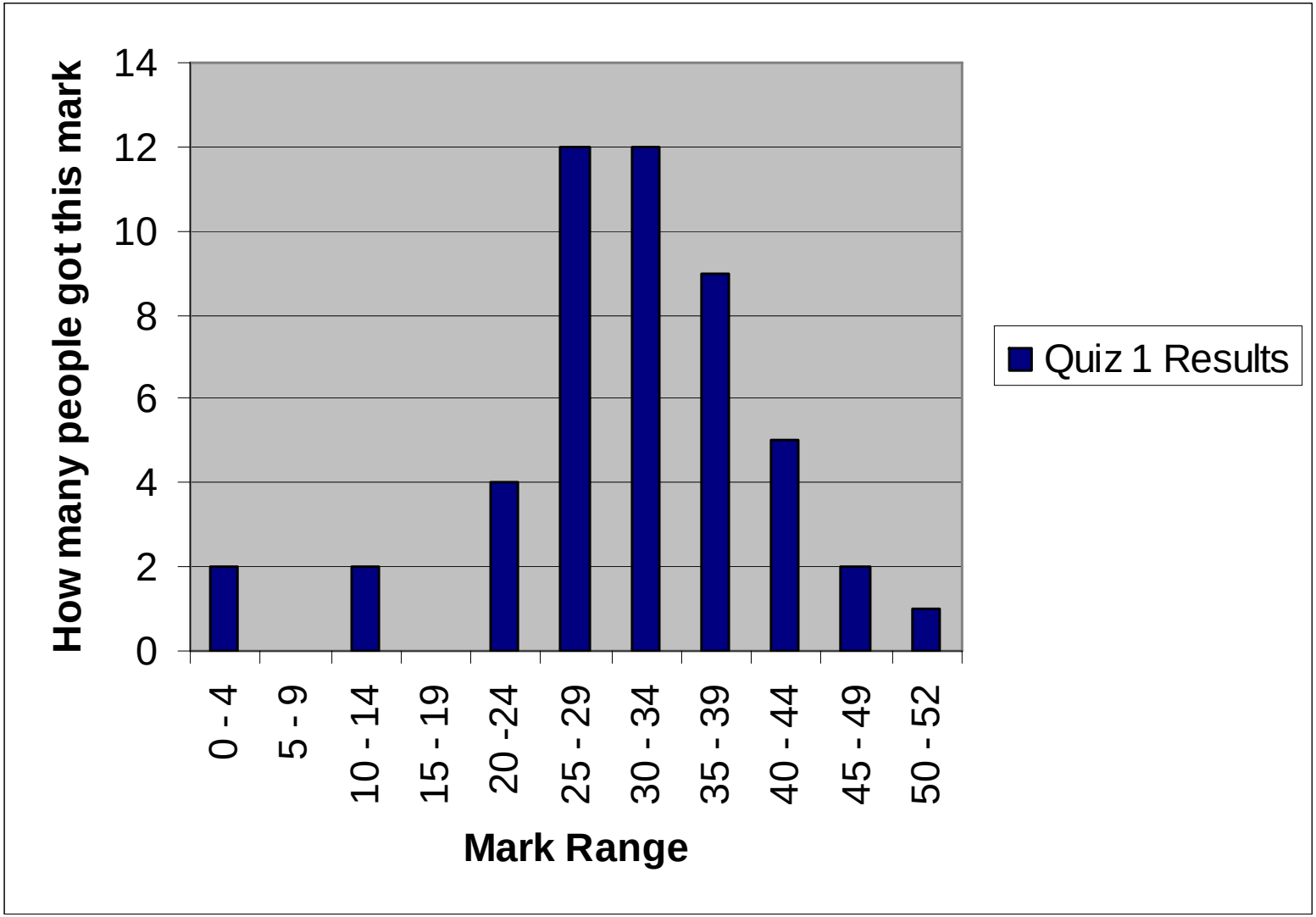
What your marks mean in terms of your final mark

• 52	7.5%
• 47	6.75%
• 42	6%
• 36.5	5.25%
• 31.5	4.5%
• 26	3.75%
• 21	3%
• 16	2.25%
• 10.5	1.5%

How everyone did do

- The “bad” questions
  - All of question 1
  - 2. (iii)
- Average
  - Mean: 31.54
  - Median: 31.5
  - Mode: 27.5
  - Std Dev: 9.98
  - Maximum: 50
  - Minimum: 3.5

How everyone did do



Answer 1.

- Three different ways to describe sequential circuits and their VHDL constructs:
  - Dataflow
    - Block and Guarded
  - Behavioural
    - Process
  - Structural
    - NAND, NOR, NOT

Answer 1.

- D-flipflop circuit implementations

Answer 1.

- Why might one choose one circuit implementation over another:
  - Power
  - Area
  - Cost
  - Timing** (not as much)

Answer 2. Synthesizable circuits – Process patterns

- Purely Combinational
  - Every input must be in the sensitivity list
  - Every output must be assigned a value for every possible combination of the inputs

Answer 2. Synthesizable circuits – Process patterns

- Purely Sequential
  - Only the clock should be in the sensitivity list
  - Only signals that change on the same edge of the same clock should be part of the same process

Answer 2. Synthesizable circuits – Process patterns

- Purely Sequential with Asynchronous Set/Reset
  - The sensitivity list includes the clock and set/reset signals
  - To ensure that the contents are registered instead of a clk'event clause must be included
  - Inside the first part of the if statement, the first assignment to the output must be either a '0' or a '1' based on the set/reset signal

Answer 2. Synthesizable circuits – Process patterns