Digital System Design

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Slide Set: 8
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Timing of Synchronous Circuits

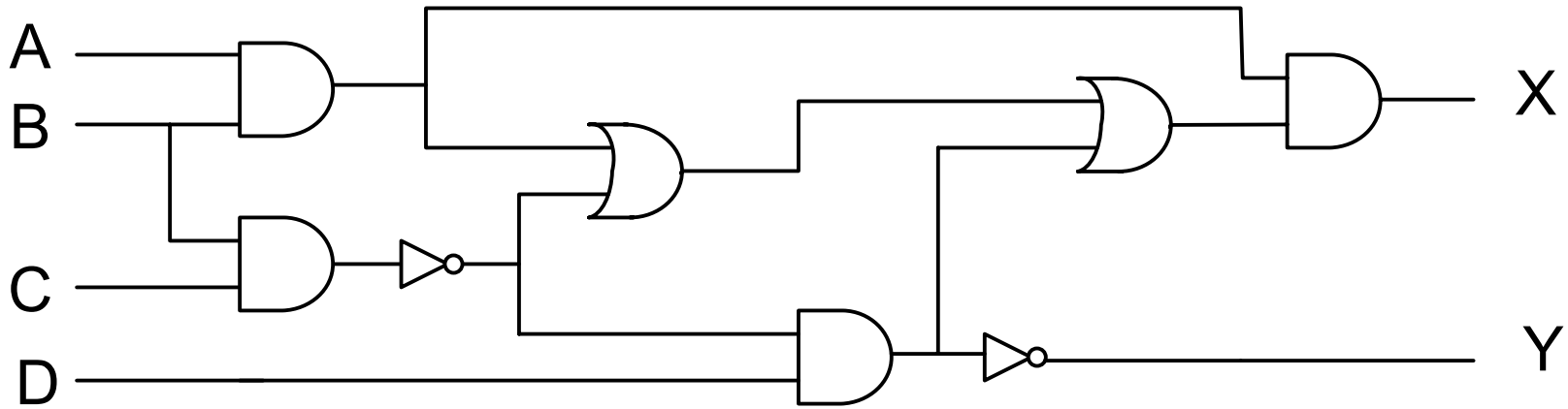
Some people seem a bit confused about the relationship between gate delay, operating frequency, and circuit topology.

This slide set should clear all that up. This is also important for datapath and ALU design, since we are concerned about the speed" of the circuits we design.

This is fairly simple stuff, and we've talked about it already in bits and pieces but this should provide a more cohesive picture

Combinational Delay

- What is the longest delay in this combinational circuit?
  - Assume the delay of each gate is 1ns



- The longest delay is the delay of the longest path between any input and any output.

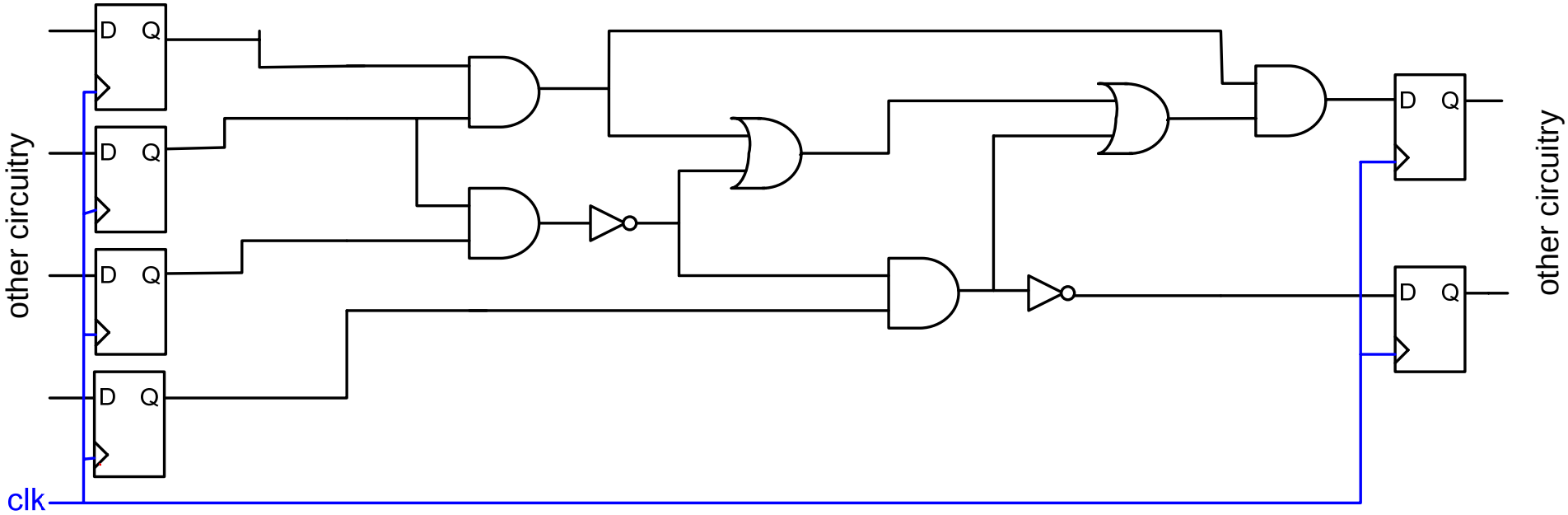
Longest delay = 5 ns

Combinational Delay

- In other words, in the previous circuit, if we apply all inputs at time 0, then by time 5, all the outputs have settled to their final values.

Notes:
1. Some outputs might settle earlier
2. Some outputs may switch back and forth a few times before settling to a final value

Add flip-flops to inputs and outputs



Clock goes from 0 to 1 at time 0. Assuming no delay in the flip-flop, the outputs of each of the first four flip-flops goes high at 0.

Some time later, the clock goes high again, and latches data into the output flip-flops. This can happen any time >= 5ns.

Circuit Delay

- In the previous slide, the minimum clock period (time between rising clock edges is 5 ns).

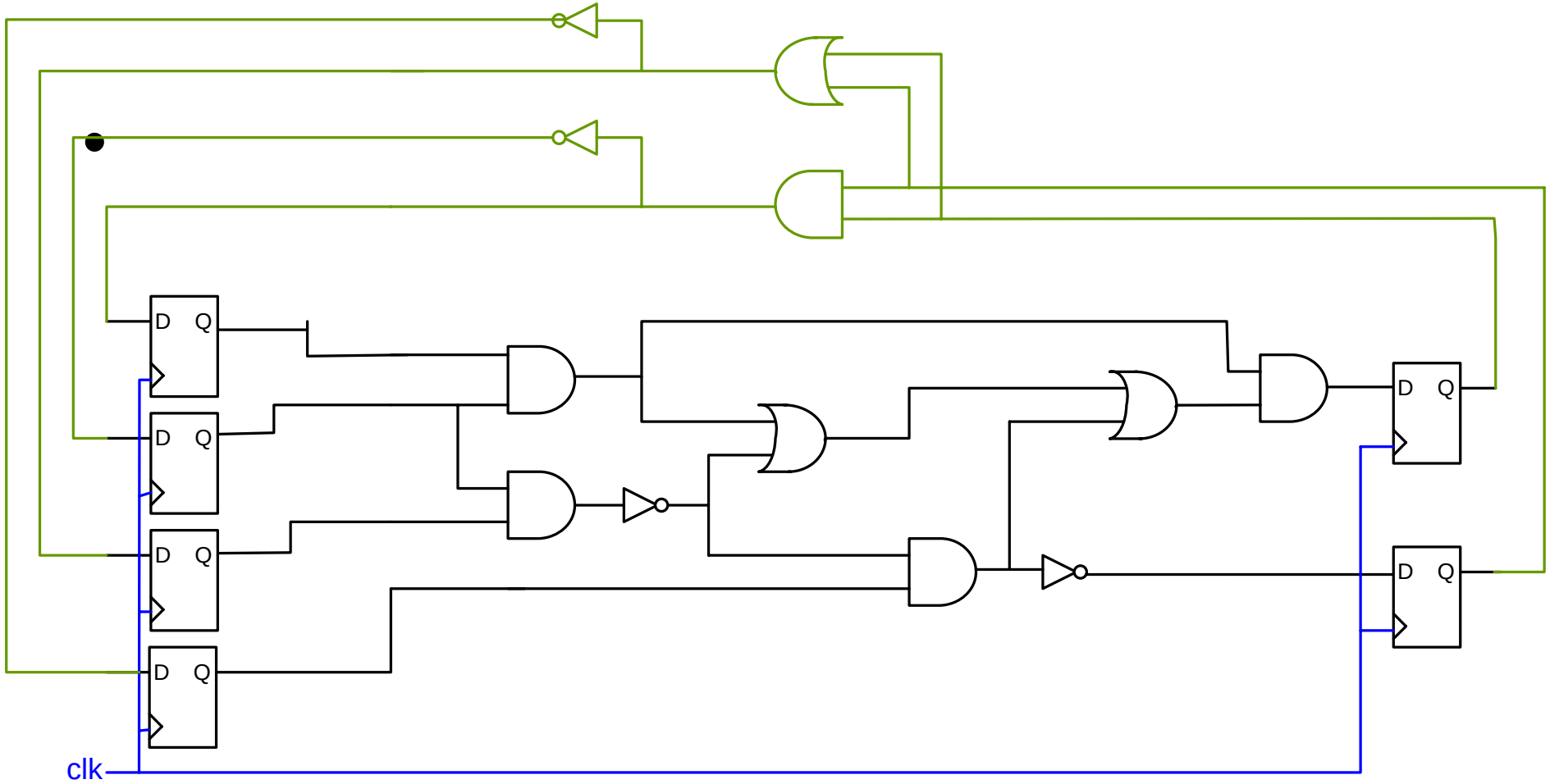
- Therefore, maximum clock frequency is

  1 / 5ns = 200 Mhz

- In general, you find the maximum delay from any flip-flop output to any flip-flop input. This path is called the ***critical path*** of the circuit.
- The delay of the critical path dictates the maximum frequency of your circuit:

  max freq = 1 / (delay of critical path)

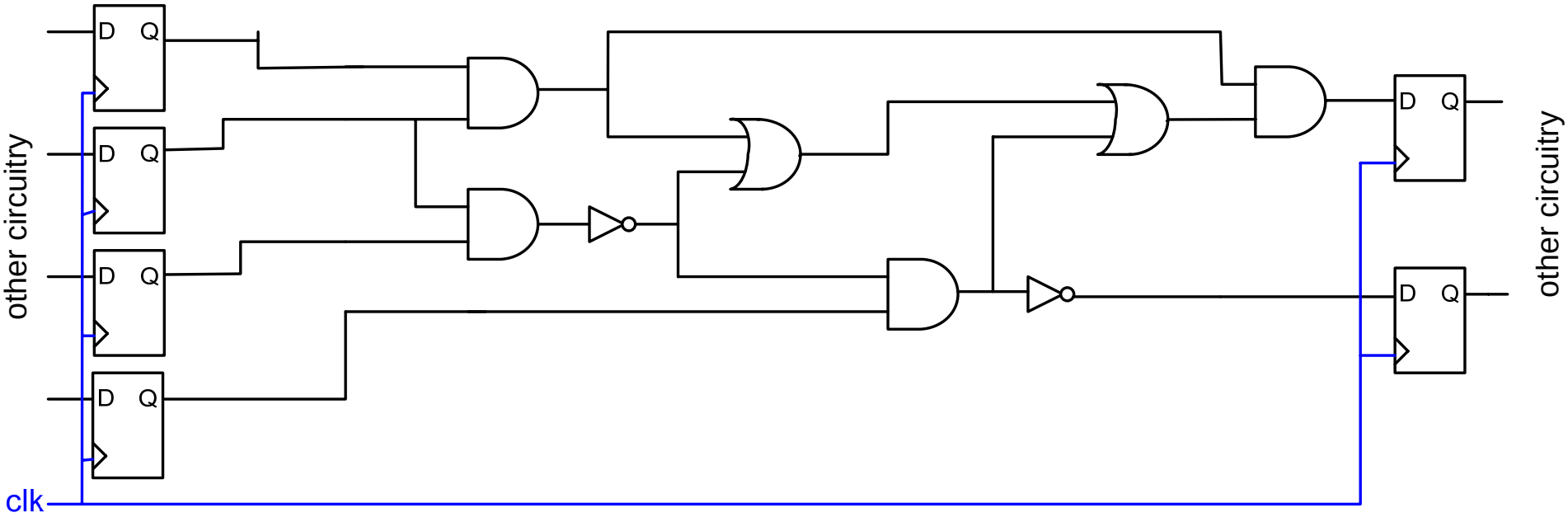
Critical Path Delay



Critical path is longest path between flip-flop output and flip-flop input.

In this case, it is 5 ns. So the maximum frequency of this circuit is 200Mhz

What happens if you run the clock slower?



Works fine. The maximum clock period is infinity (minimum frequency = 0)

So, if the maximum clock frequency is *fmax,* the circuit will work for any clock frequency between 0 and *fmax*.

Board Notes on Glitches

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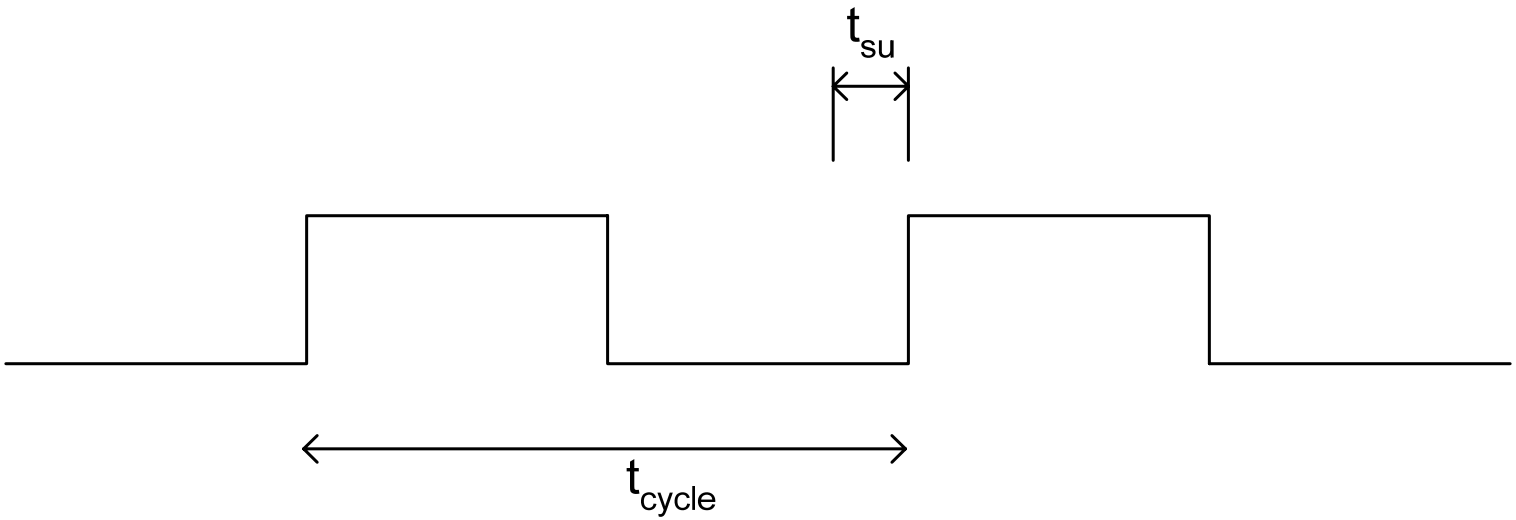
Set-Up Time

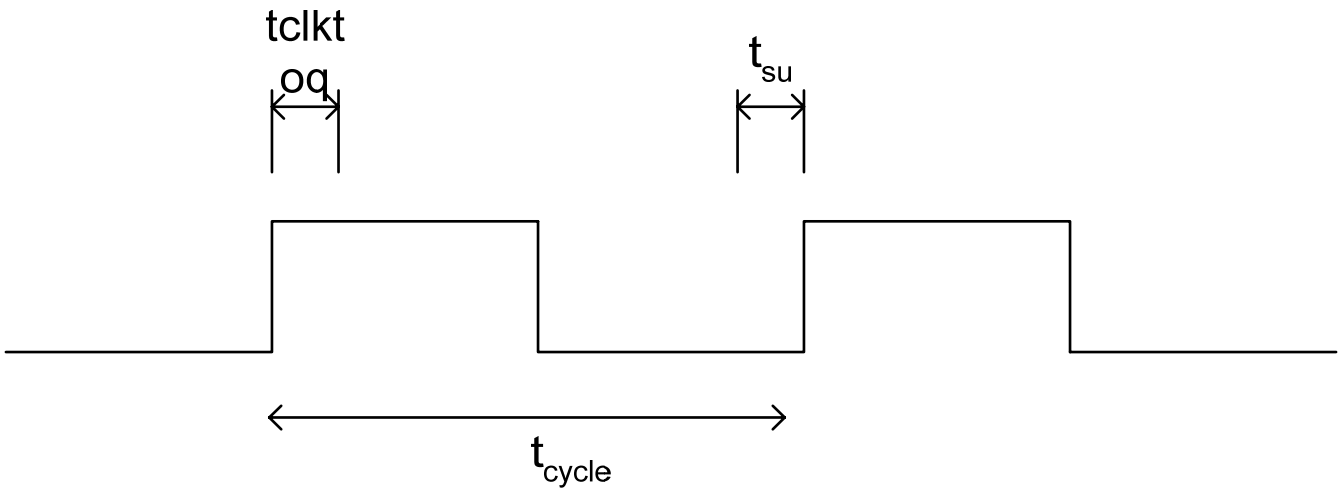
- Before, I told you that $t_{cp} <= t_{cycle}$
- But really, data must arrive at the D input of the FF a bit early



- So, more accurate to say $t_{cp} <= t_{cycle} - t_{su}$

Clk-to-Q delay of a flip-flop

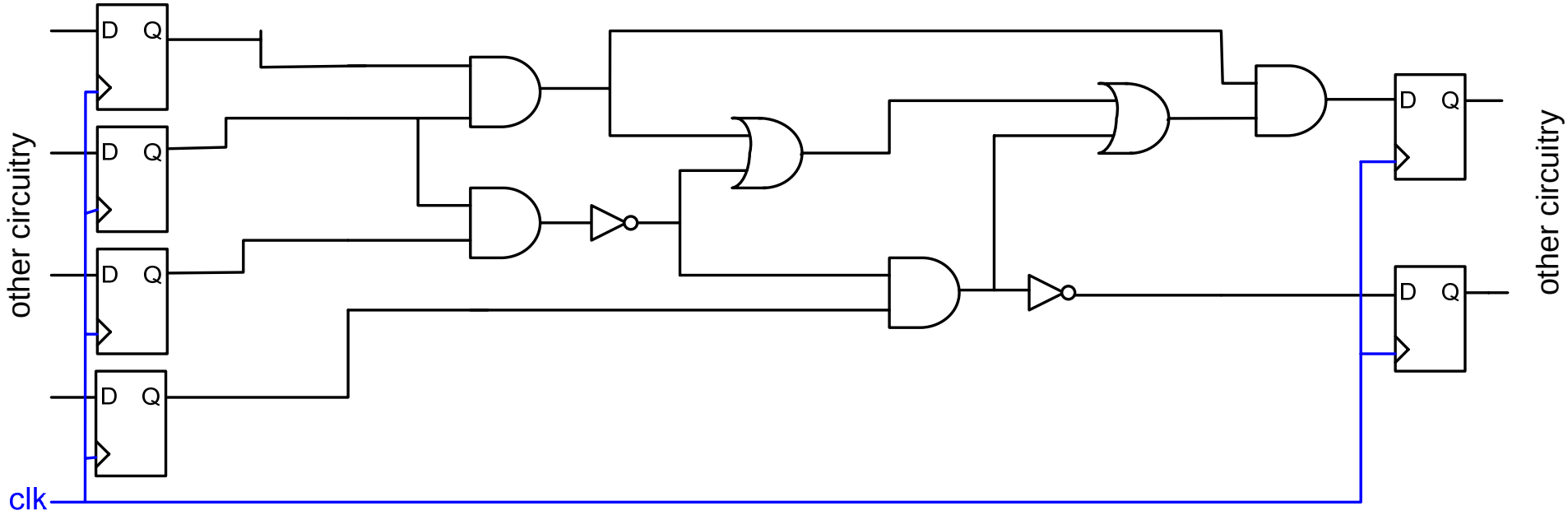
- After a rising clock edge, it takes a small amount of time, t_{clktoq}, for the output of a flip-flop to appear on Q



- So, more accurate to say $t_{cp} <= t_{cycle} – t_{clktoq} – t_{su}$

Hold time of a flip-flop

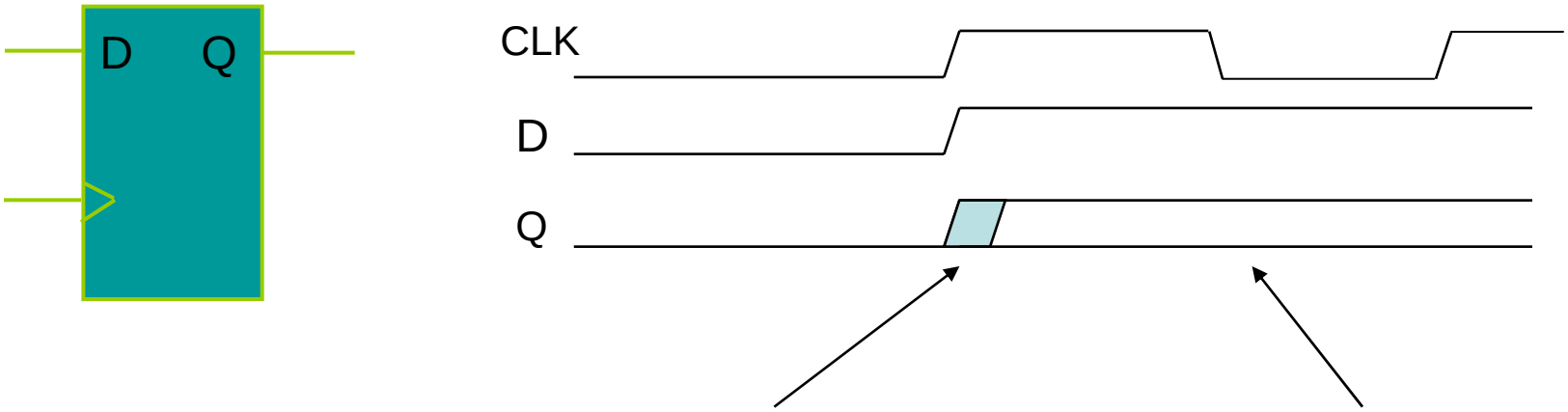
- For a short time after the rising clock edge, the D input must not change. This "short time" is denoted t_{hold}



- If the shortest delay through the combinational path is faster than t_{hold}, we might have a problem. But, this is rarely the case. Anyway, in practice, t_{hold} is often 0

Synchronous Design: Metastability

- Happens when flip flop inputs change at the same time as the clock
  - Occurs when violating setup time.
- FPGAs recovery from the metastable state quickly but the end value is indeterminate.



When a setup time is violated, METASTABILITY may occur and the end state is indeterminate

“Board” Notes on the Details of Metastability

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Summary of this slide set

- Most digital circuits operate this way:
  - Rising clock edge causes all flip-flop to produce a value on Q
  - These values propagate through combinational logic (this is the “computation” of the circuit)
  - By the *next* rising clock edge, the computation is done, and values are ready to be read into the next flip-flop

- Some systems operate differently
  - Multiple clocks for different parts of the circuit (ENSC452 and ENSC450?)
  - No clock at all (asynchronous – we’ll talk a little bit about this later in this course!)

Questions

- What is a glitch? (Be able to draw an example of how this might happen)

- Are glitches a problem? Why/Why not?

Questions

- What is another term for the longest combinational path delay in a circuit?

- Can circuits run at lower frequencies then Fmax? Why/Why not?

Questions

- What is metastability?

- What causes metastability?

Questions

- How do we prevent metastability from causing circuit failure?

- Given an even number of inverters, is it possible to achieve steady state values?