**Simon Fraser University**
**School of Engineering Science**
ENSC350: Digital System Design
Spring 2009

# ENSC 350 Altera Tutorials Guide

Last updated Jan 2nd, 2009

***Should be completed by January28th, 2009 at the latest***

The following tutorials will be made available on the course website. Complete them to familiarize yourself with the Altera tools. It is recommended that you complete the tutorials in the order listed here.

- tut_quartus_intro_vhdl.pdf
- tut_simulation_vhdl.pdf
- tut_timing_vhdl.pdf
- tut_lpms_vhdl.pdf

These tutorials were created for the Altera DE2 board and Quartus II v5.0. However, SFU has the DE2-70 board and Quartus II v7.2 Service Pack 1. Therefore, there are some sections of the tutorials that give slightly inaccurate instructions. The major changes required to adapt the tutorials are included in this document. However, there are some minor discrepancies that aren't noted. For example many of the screen shots aren't completely correct. Use your best judgment when running through the tutorials, when in doubt ask the TA and check WebCT.

To run Quartus II go to Start > All Programs > Altera > Quartus II 7.2sp1 Web Edition > Quartus II 7.2sp1 Web Edition

Other relevant files

- DE2_70_pin_assignments.csv
- addersubtractor.vhd
- addersubtractor2.vhd

# Quartus II Introduction Using VHDL Design

(tut_quartus_intro_vhdl.pdf)

Figures known to be inaccurate

| Figure | Page |
|---|---|
| 8 | 7 |
| 9 | 8 |
| 10 | 9 |
| 17 | 12 |
| 20 | 14 |
| 21 | 15 |
| 24 | 16 |
| 27 | 17 |
| 35 | 21 |
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| 41 | 25 |
| 43 | 25 |
| 44 | 26 |

## *2 Starting a New Project*

- Put the introtutorial folder in C:/temp on the SFU lab machines or on your H:/ drive. Note that all files in C:/temp are occasionally deleted, so you should save your work to a USB before logging out. Running your project off the hard drive (C:/temp) as opposed to the networked H:/ drive may improve the runtime of the Altera tools slightly.

- Chose the Cyclone II EP2C70F896C6 in the New Project Wizard: Family and Device Settings window

## *4 Compiling the Designed Circuit*

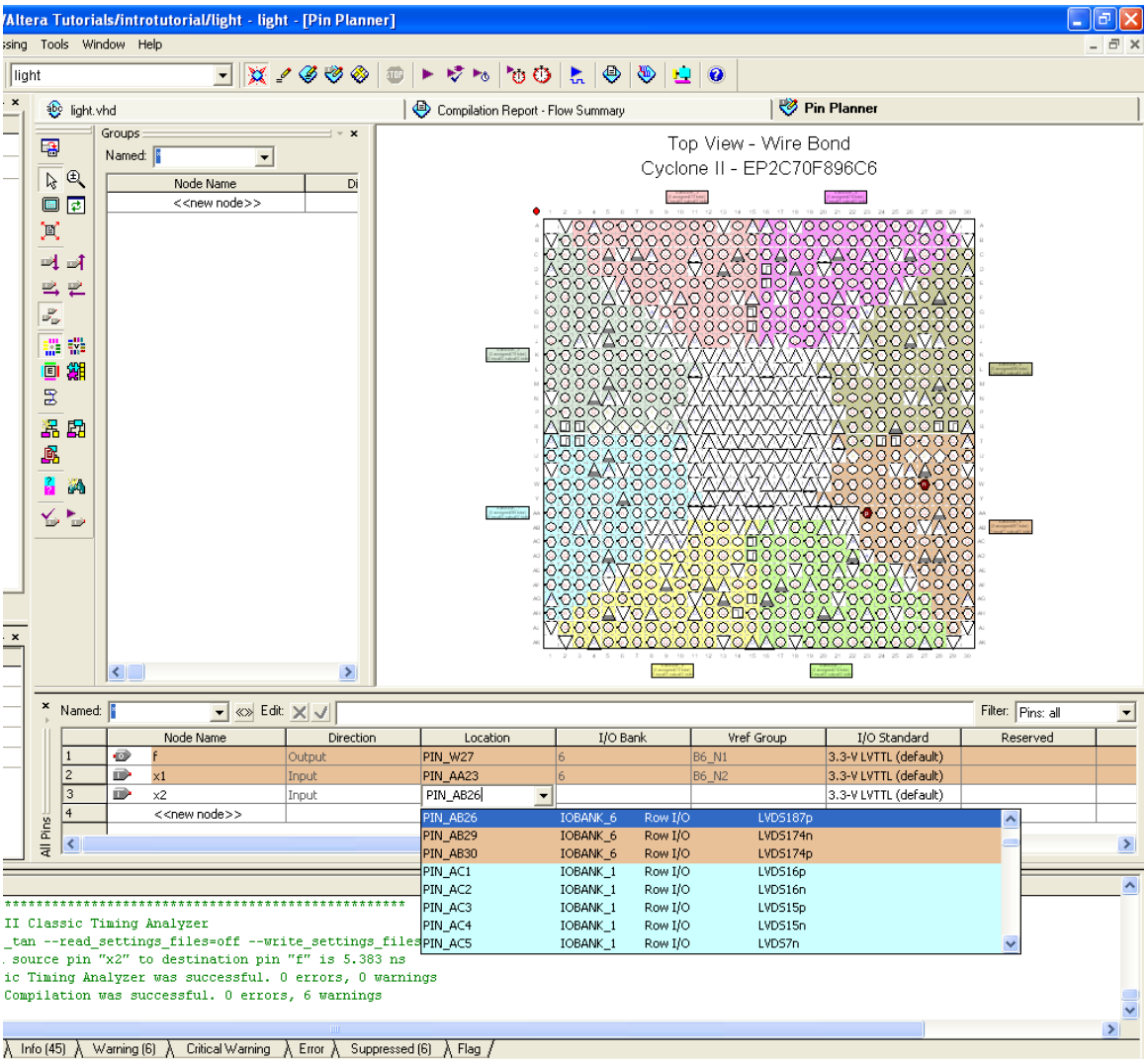
- There is not Analysis & Synthesis > Equations menu in the Compilation Report. Browse the other menu items instead.

## 5 Pin Assignment

- Correct pin assignments for the DE2-70 board. Assign these to the Location fields of f, x1, and x2 respectively.
  - LEDG0 => PIN_W27
  - SW0 => PIN_AA23
  - SW1 => PIN_AB26

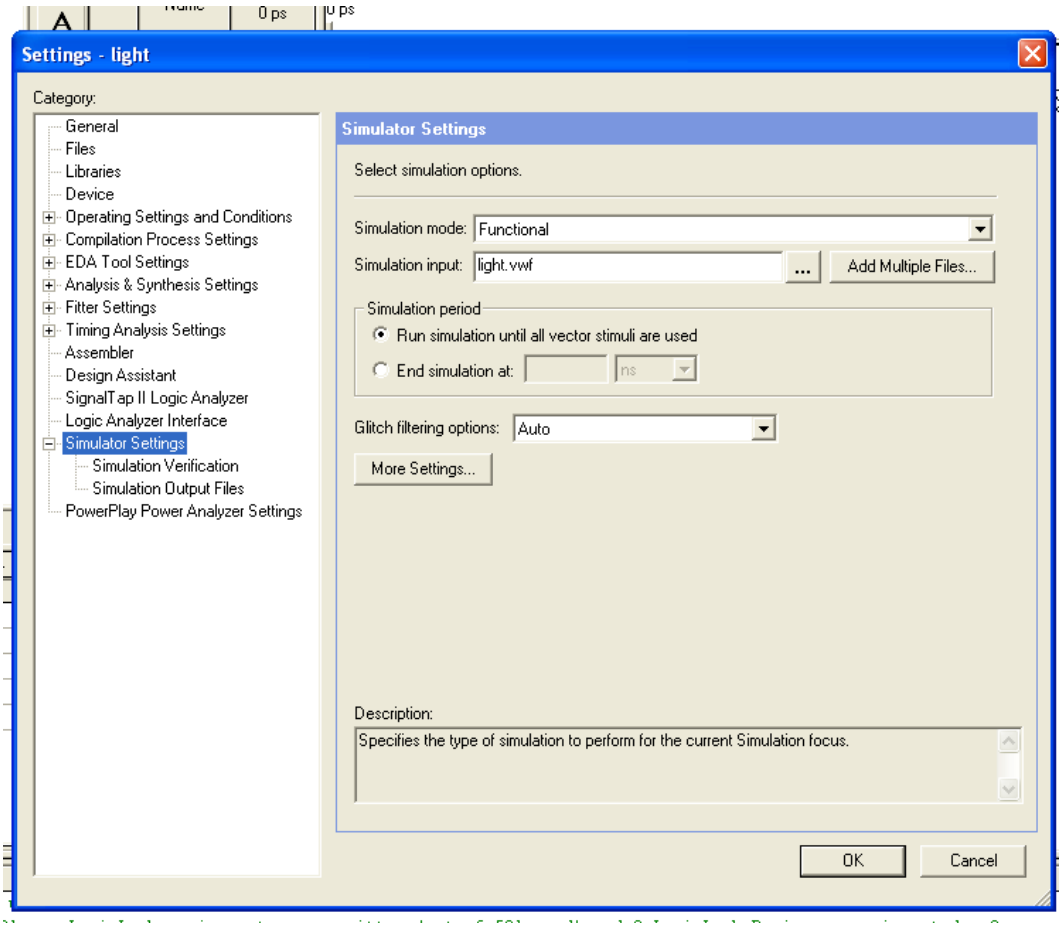
- Exporting your assignments creates a .qsf file, not a .csv file.

- New pin assignment screen




## 6.1.1 Functional Simulation

- Settings window for setting up a Functional Simulation




### *6.1.2 Timing Simulation*

- You won't see a glitch in the waveform. You can set the tool to detect glitches and generate warnings by doing
  - Processing > Simulator Tool
  - Check the Glitch Detection box in the window that pops up
  - Close the window and rerun the simulation

## *6 Programming and Configuring the FPGA Device*

- Keep the RUN/PROG switch in the RUN position. Only use the JTAG method of programming the device. You can ignore the AS mode.

- Use the device EP2C70F896

# Quartus II Simulation with VHDL Designs

(tut_simulation_vhdl.pdf)

Figures know to be inaccurate

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## *1 Example Circuit*

- Use the device EP2C70F896 when creating the project

# Timing Considerations with VHDL-Based Designs
(tut_timing_vhdl.pdf)

Figures know to be inaccurate

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| 9 | 9 |
| 11 | 10 |
| 12 | 11 |
| | |

## *1 Example Circuit*

- Use the device EP2C70F896 when creating the project

## *3 Specifying Timing Constraints*

- Set fmax by doing the following

1 Assignments > Timing Analysis Settings
2 In the window that opens select Classic Timing Analyzer Settings from the left hand menu.
3 Change the Default required fmax field tot 250
4 Recompile

# Using Library Modules in VHDL Designs

(tut_lpms_vhdl.pdf)

Figures know to be inaccurate

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- In step 7 page 9 add the following text at the end “Click NEXT” (two times NEXT)