Simon Fraser University
School of Engineering Science
ENSC350: Digital System Design
Spring 2009

Facts Sheet

Instructor:

Dr. Lesley Shannon, E-mail: lshannon@ensc.sfu.ca Office: ASB 8819
Office Hours: Mondays 10:30-12:30pm

Teaching Assistants:

David Dickin E-mail: drdickin@sfu.ca Office: ASB 8803.1
Office Hours: Tuesdays and Thursdays 2-3pm

Class:

Lecture: **Monday 8:30-10:20am, and Wednesday 9:30am-10:20pm, AQ4150**

Labs: There will be a significant lab component to this course involving HDL designs using the Altera DE2-70 boards. You will have to sign out these boards for the term. The appropriate software has been installed in Lab 1 and the new Lab 1a. Each lab group will consist of two individuals (unless specifically permitted by the instructor).

You are responsible for treating the lab equipment with proper care and respect – the same as you would any of your own possessions!! Failure to do so will affect your grade!

The Course:

This course concentrates on the skills required and challenges encountered when designing digital hardware systems. Digital hardware is becoming increasingly prevalent in society –from the computer used to write this document to the portable devices that we all carry around each and every day. Digital hardware designers are being required to implement increasingly complex circuitry. We will be using Field-Programmable Gate Arrays (FPGAs) to implement the designs for your labs and projects and will cover the architecture and programming of these devices. Upon completing this course, you should have developed some of the fundamental skills required by all hardware designers.

Course Web Page:

The course web page is at http://www.ensc.sfu.ca/~lshannon/courses/ensc350/. Handouts will be posted. I will try to post lecture notes before each lecture so that you can print them out before class. We will be using WebCT, but only for the bulletin board postings. All other material can be found from the course web page.

Course Bulletin Board:

All students *must* regularly check the course bulletin board – in other words *at least* once a day. All course related questions *must* be posted to the bulletin board; neither I nor my TAs will answer technical emails. Postings are set to be anonymous, but if you sign your name it will count towards your class participation mark (see *Mark Breakdown* and *Class Participation* below). Announcements and hints regarding the labs/projects will be posted here. I have also created a class mailing list so that last minute announcements can be sent when necessary. However, I will be the only person allowed to send to the mailing list to prevent spam. If you want to contact your fellow classmates, use the bulletin board

Textbook:

Custom Courseware copies of Douglas J. Smith's HDL Chip Design: A Pracitical Guide for Designing, Synthesizing & Simulating ASICs and FPGAs Using VHDL or Verilog are recommended for this course.

Additional Suggested HDL References Online:

Please check the course webpage for some suggestions.

Prerequisites: CMPT/ENSC 250, & ENSC215/ENSC 151

Lab Component:

The lab component will begin with tutorials that will help you to familiarize yourself with the tools. This will be followed by a series of projects that will be used to reinforce concepts introduced in lecture. People will work in lab groups of two individuals on each project. Both individuals will be responsible for all of the code and will be questioned individually on the functionality and operation of their design during its demonstration. Further details on these projects will be given in a separate handout.

Throughout the semester, students are required to follow the lab policies outlined by the School of Engineering Science along with those provided in the lab handouts. Please read them carefully.

Quizzes:

There will be two ***pop*** quizzes during the term. You will receive between three and ten days notice to prepare for each quiz.

Midterm and Final:

There will be a 110 minute in-class midterm scheduled for Monday, February 23rd and a 3 hour final that will be scheduled for Wednesday, April 15th, 2009 from 8:30am-11:30am (Room TBA).

Mark Breakdown:

- Lab Component 30 %
- Quizzes (2) 15 %
- Midterm (Feb 23rd) 20 %
- Final Exam 35 %
- Class Participation ***Bonus*** 5 %

Class Participation:

Finally, I feel that it is important that people work together – they learn more. In a design team, everyone needs to contribute to the group. That means speaking up when there's a problem or when you see a solution. Although the Bulletin Board will not be marked, good "citizenship" demonstrated through in-class participation, in-lab cooperation, and asking and answering each others questions on the bulletin board will be rewarded with a maximum of a ***5% bonus*** on a student's final mark.

Topics:

- Field Programmable Gate Array architecture and technology (Altera, Xilinx)
- Hardware Description Languages and Simulation (possibly synthesis)
- Advanced state machine concepts
- Digital design techniques
- An introduction to floating point arithmetic architecture
- Digital signal processing algorithm implementation
- Design for high performance digital systems
- Computer bus interfacing

*****Important Notes***: While I promote team work and helping each other, code copying and plagiarism will ***NOT*** be tolerated. Any individual found copying code from other class members or the web will receive an automatic ***0*** on the ***entire*** lab component. Similarly, anyone found copying during quizzes, midterms, or the final will receive a ***0*** for the ***entire*** testing component. Any code copying or plagiarism will result in an automatic ***0*** for the class participation bonus.